GTE-ERS
TECHNICAL LIBRARY
04914

MODEL 7046

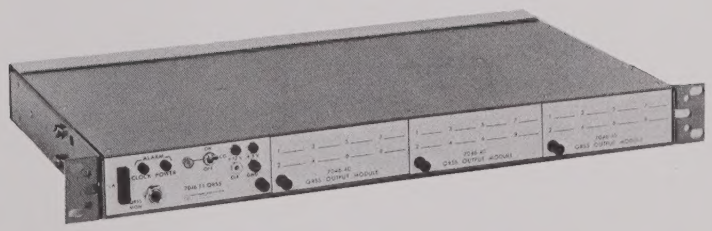
PCM QRSS GENERATOR

Northeast Electronics Instruction Manual
A7046-00-600 Issue 2 January 1978

tau-tron
A UNIT OF
GENERAL SIGNAL

MODEL 7046

PCM QRSS GENERATOR



Northeast Electronics Instruction Manual
A7046-00-600 Issue 2 January 1978

tau-tron
A UNIT OF
GENERAL SIGNAL

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_11097

NOTICE

PLEASE DISREGARD THE WARRANTY AND SERVICE INFORMATION CONTAINED IN OTHER SECTIONS OF THIS MANUAL. TAU-TRON'S *NEW 3-YEAR WARRANTY* AND SERVICE INFORMATION ARE LOCATED IN THE FRONT OF THIS MANUAL AND NOW APPLY TO ALL TAU-TRON AND NORTHEAST ELECTRONICS PRODUCTS.

– WARRANTY –

ALL TAU-TRON TEST SETS ARE WARRANTED AGAINST ANY DEFECTS IN MATERIAL AND WORKMANSHIP, FOR A PERIOD OF *3 YEARS.*

This Warranty applies from the date of delivery for all Tau-tron test sets. Other manufacturers products offered by Tau-tron such as printers, cables, etc. are covered to the extent of their own warranty. Calibration of Tau-tron test sets is covered for 1 year from date of delivery. However, some restrictions apply; see your salesman for further details.

We will repair or replace test sets which, upon our examination, prove to be defective during the warranty period, except in cases of product abuse or attempted field repair.

No other Warranty, expressed or implied, including fitness for purpose, merchantability or otherwise, is given.

For assistance, contact Customer Service with details of the instrument model, serial numbers, and malfunction; see Repair Returns below.

SHIPPING DAMAGE

If any signs of damage are noticed on the outside of the carton, make a request for the carrier's agent to be present during unpacking. If external damage is found on the instrument, follow Repair Returns procedure below.

Check the electrical performance of the instrument as soon as possible after receipt. If there are any malfunctions, follow Repair Returns procedure below.

REPAIR RETURNS

For mechanical damage or electrical malfunctions, notify Tau-tron immediately. If the damage occurred during shipping, also notify the carrier. To return a unit for repair:

1. Call the Customer Service Department, **(508) 692-5100** (800-TAU-TRON [800-828-8766], outside MA), for a **Repair Authorization Number**. The use of this number reduces administrative delays and ensures the prompt return of your unit.
2. Complete and **attach the Repair Tag**, located in the back of the manual, **to your unit** for positive identification.
3. Pack the unit in the original shipping carton and packing materials, if available. Otherwise use a double-walled carton (test strength of 350 lb; 159 kg) and shock-absorbing material such as bubblewrap, to prevent the unit from moving in the carton during transit. Secure the carton by sealing with heavy paper tape.
4. Send to: Tau-tron Inc.
   10 Lyberty Way
   Westford, MA 01886
   Attn: Customer Service

TABLE OF CONTENTS

SECTION	TITLE	PAGE
1	**DESCRIPTION**	1–1
	1.3 7046 Common-Equipment Module	1–1
	1.7 7046-40 Output Module	1–1
2	**SPECIFICATIONS**	2–1
3	**INSTALLATION**	3–1
	3.2 Initial Inspection	3–1
	3.4 Return Material Authorization	3–1
	3.6 Removing The Shield	3–1
	3.8 Rack Mounting	3–1
	3.10 Installation Wiring	3–1
4	**OPERATION**	4–1
	4.2 Controls,Indicators, and Jacks	4–1
	4.4 Operation	4–1
5	**THEORY OF OPERATION**	5–1
	5.2 Overall Block diagram Description	5–1
	5.4 Common Equipment Module	5–1
	5.13 Output Module	5–1
	5.16 Common Equipment Module Detailed Circuit Description	5–2
	5.18 Oscillator And Clock Generator	5–2
	5.21 QRW Generator	5–2
	5.24 15 And 20 Zero Detectors	5–2
	5.30 Single Rail-To-Double Rail Converter	5–4
	5.33 Bipolar Output Number 1	5–4
	5.36 Group Shift Registers	5–4
	5.38 Alarm Circuits	5–5
	5.44 Power Supplies	5–5
	5.46 Output Module Detailed Circuit Description	5–5
	5.48 +6 VDC Power Supply	5–5
	5.50 Ø Clock Generator	5–5
	5.53 Shift Registers	5–6
	5.55 Bipolar Outputs	5–6
6	**CALIBRATION**	6–1
	6.2 Clock Frequency Calibration	6–1
	6.4 Output Number 1 Level Calibration	6–1
	6.6 Output Module Level Calibration	6–1
7	**DIAGRAMS**	7–1
8	**PARTS LISTS**	8–1

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
2–1	Model 7046 Output Waveform	2–2
3–1	Protective Shield Shown Mounted On The Mainframe	3–2
3–2	Model 7046 Dimensional Outline Drawing	3–3
3–3	Installation of Rack Mounting Adapters	3–4
3–4	Mainframe Installation Wiring Terminals	3–4
4–1	Model 7046 PCM QRSS Generator Series Controls, Indicators and Jacks	4–2
5–1	Model 7046 Functional Block Diagram	5–3
5–2	Oscillator And Clock Generator Timing Diagram	5–2
5–3	15 Zero Detector Timing Diagram	5–4
5–4	Single Rail-To-Double Rail Converter Timing Diagram	5–4
5–5	Bipolar Output No. 1 Timing Diagram	5–4
5–6	Group Shift Registers Timing Diagram	5–5
5–7	Ø Clock Generator Timing Diagram	5–5
5–8	Shift Register Timing Diagram	5–6
6–1	Model 7046 Clock Frequency Calibration Typical Test Setup	6–1
6–2	Model 7046 Output Level Calibration Typical Test Setup	6–1
6–3	Model 7046 Calibration Adjustment Locations	6–2
7–1	Model 7046 QRSS Generator Interconnection Diagram	7–3
7–2	Common Logic Board A1, Component Location	7–4
7–3	Power Supply Board A2, Component Location	7–4
7–4	7046 Common Equipment Module Schematic Diagram	7–5
7–5	7046-40 Output Module, Component Location	7–6
7–6	7046-40 Output Module, Schematic Diagram	7–7

LIST OF TABLES

TABLE	TITLE	PAGE
2–1	Specifications	2–1
4–1	Controls, Indicators, And Jacks	4–1
8–1	Common Equipment Module Overall Parts List	8–1
8–2	Common Logic Board A1 Parts List	8–2
8–3	Power Supply Board A2 Parts List	8–3
8–4	Mother Board Parts List	8–3
8–5	Output Module Parts List	8–3

SECTION 1

DESCRIPTION

1.1 The Northeast Electronics 7046 series of PCM QRSS Generator equipment can provide up to 25 quasi-random DS-1 signals. These signals will normally be used to drive spare LD-1/T1 span lines, but can be used as general-purpose test signals as well.

1.2 The 7046 series consists of a mainframe, a 7046 common-equipment module, and up to three 7046-40 output modules. All input/output connections are made via wire wrap terminals located at the rear of the mainframe.

1.3 7046 COMMON-EQUIPMENT MODULE.

1.4 The common-equipment module generates a basic QRW (Quasi-Random Word) signal. An internal 1.544 MHz clock generates the QRW that is 1,048,575 bits in length and is limited to 14 successive zeros. This is the Bell System standard signal used to simulate the energy spectrum of a normal LD-1/T1 bit stream.

1.5 The common-equipment module provides one QRSS output via wire wrap terminals at the rear of the mainframe. It also provides two sets of form C contacts for use by remote alarm equipment, such as an external audible alarm.

1.6 Located on the front panel are indicators and test jacks for determining the operating status within the module. The indicators turn on when either the clock or one of the power supplies fails. To silence the audible alarm system, an ACO (Alarm Cutoff) switch is provided. As a reminder that the audible alarm system has been disabled, an ACO indicator is lighted. Test points monitor the basic clock, the QRSS output, and the power supplies.

1.7 7046-40 OUTPUT MODULE.

1.8 Up to three output modules can be plugged into the mainframe, making up to 24 additional QRSS outputs available for use via wire wrap terminals at the rear of the mainframe. Each successive output (starting with the common-equipment output) is offset from its adjacent output by one clock pulse period of 648 nanoseconds. Altogether, a total of up to 25 outputs can be used.

1.9 The front panel of each output module is covered with an overlay that can be written on with pencil. Space for recording eight output assignments is provided on the front panel of each module.

1.10 Universal adapters are provided so that the mainframe can be mounted in either a 19-inch (48.3cm) or a 23-inch (58.4cm) rack. The adapters can also be oriented on the mainframe so that the front panel is flush with the mounting rack or protrudes 4 inches (10.2cm) in front of the rack.

1.11 The mainframe measures 17 inches (43.2cm) wide by 1-¾ inches (4.5cm) high by 10-½ inches (26.7cm) deep. It weighs approximately 6-¾ pounds (3.1kg) when three output modules are used. Power consumption is approximately 19 watts at 48 Vdc. The input power line is fused at ½ Ampere.

SECTION 2

SPECIFICATIONS

2.1 This section contains the specifications for the 7046 series of PCM QRSS Generator equipment.

Table 2—1. Specifications.

QRSS Characteristics	
Quasi-random Word Format:	Standard Bell System pattern of 1,048,575 bits with a maximum of 14 successive zeros.
Clock Frequency and Accuracy:	1.544 MHz ±0.005%.
Clock Frequency Temperature Stability:	$\pm 30 \times 10^{-6}$ from 0°C to +50°C.
Pulse Width:	324 nanoseconds ±10% for both positive and negative pulses, at the 50% points.
Pulse Width Unbalance:	Positive and negative pulse widths are equal within ±15 nanoseconds. Both are also within pulse width specification.
Rise and Fall Times:	80 nanoseconds maximum from the 10% to the 90% points.
Pulse Amplitude:	3 volts peak (or 6 volts peak-to-peak) ±10% into 100 ohms.
Pulse Amplitude Unbalance:	Positive and negative pulse amplitudes are equal within ±0.15 volt. Both are also within pulse amplitude specification.
Pulse Overshoot:	10 to 30% of positive pulse amplitude.
Output Impedance:	100 ohms ±10% balanced (all outputs).
QRW Offset:	Each of the up to 25 outputs is delayed from the preceeding one by one clock period of 648 nanoseconds. The rear panel QRSS output of the common equipment module is the reference output and is defined as the number 1 output. The remaining outputs advance in number from left to right as viewed from the front panel.
MON Jack Output:	Monitors QRSS output of Common Equipment Module. 430-ohm resistors are in series with the tip and ring. The output level is compatible with standard error detectors.
Input/Output connections:	All rear panel connections are made via wire wrap terminals suited for 22 or 24 gauge wire.
Input Power:	42 to 56 Vdc. Fused at ½ Ampere.
Environmental	
Temperature Range:	0°C to +50°C.
Relative Humidity:	0 to 95% noncondensing.
Alarm Contacts:	Two sets of form C contacts are provided.

Table 2—1. (Cont'd)

Size:	17 in. (43.2cm) wide x 1-¾ in. (4.5cm) high x 10-½ in. (26.7cm) deep. Universal mounting adapters provided for 19-in. (48.3cm) and 23 in. (58.4cm) rack mounting. The mounting adapters can be situated for flush mounting of the front panel or so that the front panel protrudes 4 in. (10.2cm) to the front.
Weight:	6.75 pounds (3.2kg), including three output modules.

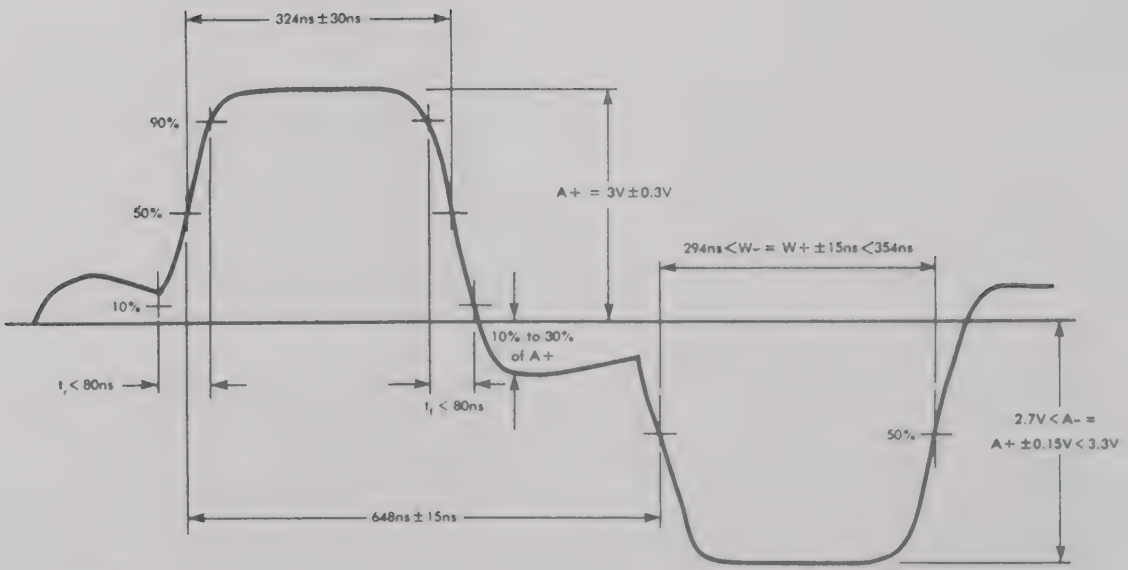


Figure 2—1. Model 7046 Output Waveform.

SECTION 3

INSTALLATION

3.1 This section provides the instructions and illustrations needed to remove the shield, install, and wire-up the 7046 series. Figure 3—1 shows the shield and Figure 3—2 is an outline drawing of the equipment. Figure 3—3 shows how to install the mounting adapters. Figure 3—4 identifies the input/output terminals.

3.2 INITIAL INSPECTION.

3.3 The Model 7046 was carefully inspected, both mechanically and electrically, before shipment. It should be free of defects and should be operating correctly when received. To confirm this, the set should be visually inspected for signs of damage that may have occurred during shipment. If there is shipment damage, notify the carrier immediately.

3.4 RETURN MATERIAL AUTHORIZATION.

3.5 As detailed on the back side of the sales agreement, Northeast Electronics warrants its instruments for a period of one year to the original purchaser. Before returning any piece of equipment to the factory for repair, a return material authorization number must be obtained from Northeast Electronics. To obtain this authorization, telephone the Customer Service Department at (603) 228-3700.

3.6 REMOVING THE SHIELD.

3.7 The Model 7046 mainframe is shipped with a protective shield mounted over the wire wrap terminals at the rear of the unit. As shown on Figure 3—1, the shield is a U-shaped bracket held in place with two screws on the top and two screws on the bottom. Remove these four screws, then remove and discard the shield. Replace the four screws in the top and bottom covers.

3.8 RACK MOUNTING.

3.9 Select either the 19-inch (48.3cm) or the 23 inch (58.4cm) orientation for the mounting adapters and bolt them to the mainframe. See Figure 3—4 for installation details concerning the adapters. Install the mainframe in the equipment rack and secure.

3.10 INSTALLATION WIRING.

3.11 At the rear of the common equipment module, connect the power input, alarm contacts, and the tip and ring of QRSS output number 1 if required. See Figure 3—4 for wiring information.

NOTE

If QRSS output number 1 is not used, connect a 100-ohm ¼ w resistor across the tip and ring terminals.

3.12 At the rear of the output modules, connect to the number of QRSS outputs required. The maximum allowable connection length of number 22 gauge cable is 250 feet.

NOTE

Terminate all unused QRSS outputs with 100-ohm, ¼ w resistors.

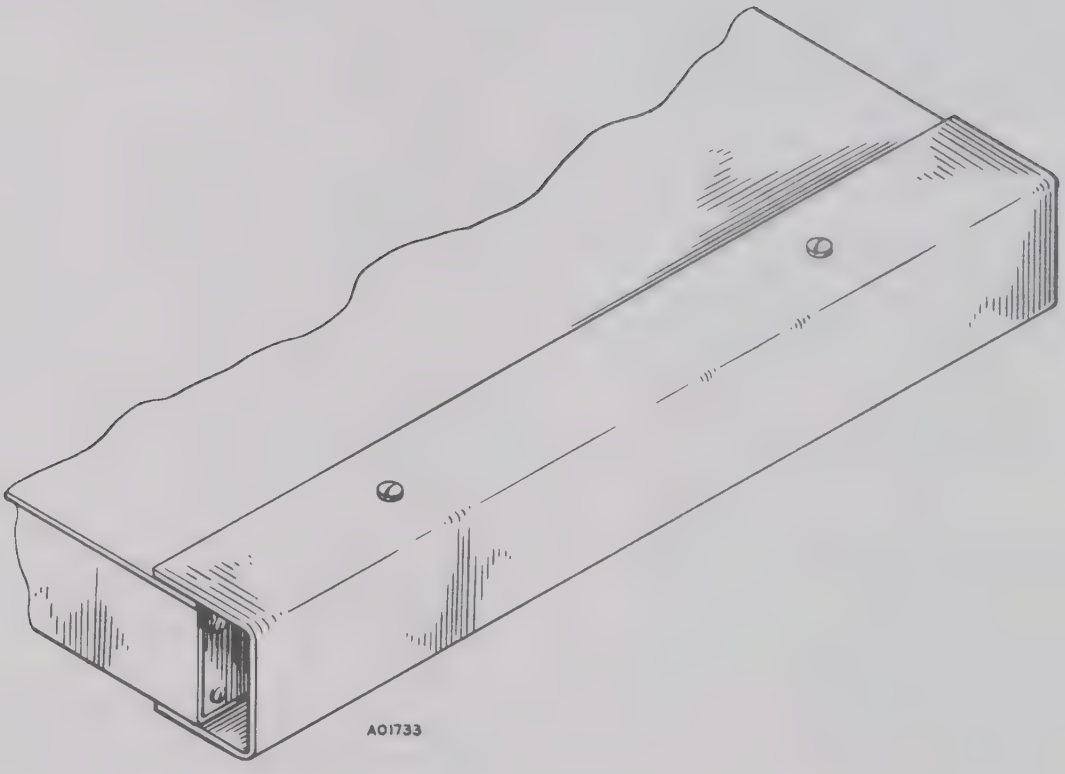


Figure 3—1. Protective Shield Shown Mounted On Mainframe.

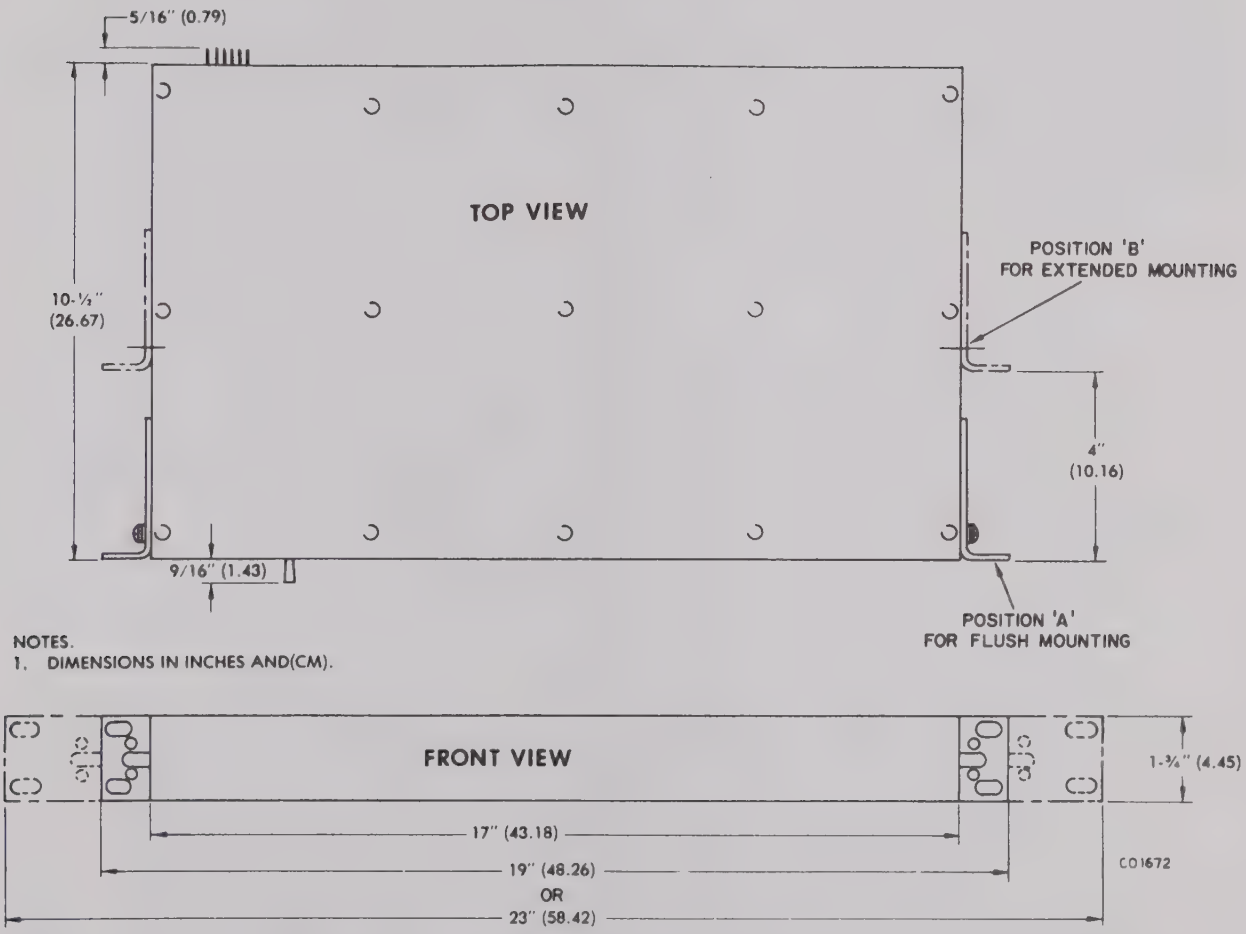


Figure 3—2. Model 7046 Dimensional Outline Drawing.

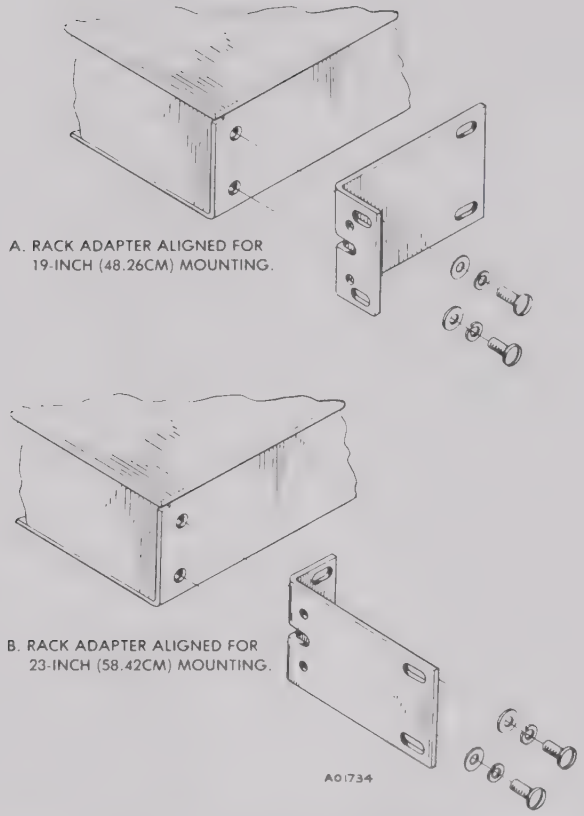


Figure 3—3. Installation of Rack Mounting Adapters.

NOTE:

ALARM CONTACTS 1-2 NO,
2-3 NC, 4-5 NO, 5-6 NC.
THIS IS FOR NON-ALARM
CONDITION.

Figure 3—4. Mainframe Installation Wiring Terminals

SECTION 4

OPERATION

4.1 This section provides operating information for the 7046 series of PCM QRSS Generator equipment.

4.2 CONTROLS, INDICATORS, AND JACKS.

4.3 Table 4—1 lists the controls, indicators, and jacks shown on Figure 4—1.

4.4 OPERATION.

4.5 Once the 7046 series of equipment is installed and wired, no further operating instructions are required. If either the CLOCK or the POWER indicators is lighted, the external alarm system should be activated. To silence the alarm system while the source of trouble within the 7046 equipment is being located and repaired, set the ACO switch to the ON position. This lights the ACO indicator to warn personnel that the switch must be returned to the OFF position to restore the alarm feature.

Table 4—1. Controls, Indicators, and Jacks.

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
DS1	CLOCK ALARM indicator	When turned on, indicates that the clock generator is not operating.
DS2	POWER ALARM indicator	When turned on, indicates that either fuse F1 is blown or one of the power supplies is not operating.
DS3	ACO indicator	When turned on, indicates that S1 is set to the ON position and the alarm system associated with the 7046 is disabled.
F1	½ A fuse	Provides protection for the 48 Vdc source.
J1	QRSS MON jack	A 310 access point to monitor the QRSS bit stream. Suitable for use with error detectors.
J2	+5V test point	A pin jack access point to monitor the output of the +5 Vdc power supply.
J3	+12V test point	A pin jack access point to monitor the output of the +12 Vdc power supply.
J4	GND test point	A pin jack to provide a ground reference for J2,J3, and J5.
J5	CLK test point	A pin jack access point to monitor the output of the basic 1.544 MHz clock generator.
S1	ACO ON/OFF switch	When set to the ON position, the ACO lamp is lighted and the external audible alarm system associated with the 7046 is disabled. When set to the OFF position, the external audible alarm system is active.

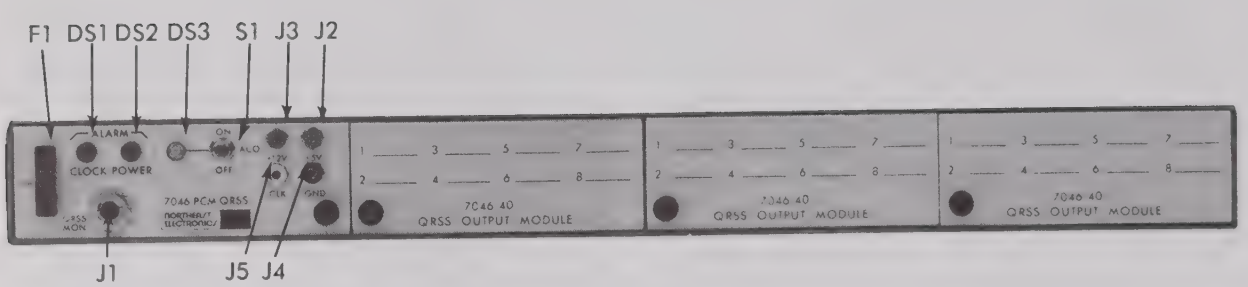


Figure 4—1. Model 7046 PCM QRSS Generator Series Controls, Indicators and Jacks.

SECTION 5

THEORY OF OPERATION

5.1 This section provides an overall block diagram description and detailed circuit level descriptions for the 7046 series of equipment.

5.2 OVERALL BLOCK DIAGRAM DESCRIPTION.

5.3 See Figure 5—1 for a functional block diagram of the unit. As shown on the illustration, the unit is basically comprised of a common equipment module and up to three output modules.

5.4 COMMON EQUIPMENT MODULE

5.5 A stable crystal oscillator operating at 6.17 MHz generates the basic signal for the QRSS (Quasi Random Signal Source). Clock pulse streams at various phases operating at the DS-1 rate of 1.544 MHz are furnished by the clock generator and used throughout the remainder of the unit.

5.6 The circuit used to generate the QRW (Quasi Random Word) is comprised of a 20-bit shift register, a 15 zero detector, a 5 zero detector, and other logic gates. When bits b_{17} and b_{20} at the output of the shift register are fed back to the serial input through an exclusive OR gate, the standard Bell System quasi random word is present in bit b_{20}. The word length is 1,048,575 bits and is limited to 14 successive zeros. Under normal operating conditions, the output of U8B is low, thus allowing b_{17} and b_{20} present at the output of exclusive OR gate U4A to simply pass through U4B.

5.7 When power is first applied to the unit, it is possible that all 20 outputs of the shift register could come up low. This would prevent the shifting of a logical 1 into the shift register from ever occurring. In effect, the generator would come to a permanent halt. To prevent this condition from happening, the outputs of the 15 and 5 zero detectors go high at 20 zeros. These are ANDED together in U8B and its high output is applied to exclusive OR U4B. Since both b_{17} and b_{20} are low at this time, the output of U4A is low. Thus a logical 1 is forced into the serial input of the shift register. This ensures that 17 bits later a logical 1 appears at b_{17}, thus starting continuous operation.

5.8 The 15 zero detector also performs the additional task of limiting the QRW to a maximum of 14 successive zeros. During normal operation, it is possible that the shift register output at b_{20} can contain strings of zeros up to 19 bits long. When 15 or more zeros are detected, the output of the 15 zero detector goes high to force the output of exclusive OR U4C to a logical 1. This condition exists until the number of zeros detected drops below 15.

5.9 The QRW present at the output of U4C is formatted such that all ones are of the same polarity. This is referred to as a unirail bit stream. The DS-1 signal however, must be formatted such that alternate ones are of opposite polarity. The first step in this process is to convert the unirail bit stream into two individual bit streams in a unirail-to-double rail converter. This produces two bit streams with alternate ones appearing in each.

5.10 The double rail signal is then applied to a bipolar driver and to two series of shift regiters. The bipolar driver, in conjunction with pulse transformer T1, produces a true bipolar signal at output number 1 of the unit. This signal is also available for test purposes at QRSS MON jack J1. The two groups of two shift registers each generate three double rail bit streams. Each bit stream is offset from the adjacent one by eight time slots. These are then applied to the three output modules.

5.11 Front panel alarm indicators and relay contacts provide the required alarm functions. When either the +5-volt or the +12-volt power supply fails, detectors sense this fact and light POWER ALARM indicator DS2. This also causes relay K1 to be deenergized. Two sets of transfer contacts are available for use by remote alarm equipment such as an external audible alarm. If the basic clock system should fail, the loss-of-clock detector, through the lamp driver, lights CLOCK ALARM indicator DS1.

5.12 The other major function performed by the common equipment module is that of generating the operating voltages required by the unit. This is performed by the +5 and +12 volt power supplies on A2. The outputs of both of these supplies are available for testing at front panel jacks J2 and J3. Ground jack J4 provides the reference for all the other jacks.

5.13 OUTPUT MODULE.

5.14 Up to three identical output modules can be used to provide up to 24 additional QRSS outputs. The double rail data supplied by the common logic module is applied to 8-bit shift registers. The Q_A output is delayed one time slot (648 nanoseconds) with respect to the serial input, the Q_B two time slots, etc. The eight shift register

outputs are then applied to a series of eight bipolar drivers that generate the bipolar signals at the outputs of the pulse transformers.

5.15 Basic timing for the shift registers and the bipolar drivers is provided by the Ø clock generator. If the clock should fail, a loss-of-clock detector sets the Ø clock generator output such that the bipolar drivers are all in their low-current state as a protective measure.

5.16 COMMON EQUIPMENT MODULE DETAILED CIRCUIT DESCRIPTION.

5.17 See Figure 7—4 for the schematic diagram of the 7046 Common Equipment Module.

5.18 OSCILLATOR AND CLOCK GENERATOR.

5.19 The crystal oscillator is comprised of Q8, 6.176 MHz crystal Y1, and bias components. Variable capacitor C1 allows the oscillator frequency to be adjusted over a limited range. The waveform at TP1 does not have the fast rise times required to drive TTL logic, so Q9 speeds up these rise times to be compatible with the TTL logic that follows.

5.20 See Figure 5—2 for the timing diagram. The necessary clock waveforms are generated by a series of three flip flops. The 6.176 MHz waveform present at TP2 is first divided by 2 in U17A to obtain a frequency of 3.088 MHz. The signal at the $\overline{Q}$ output is inverted and buffered by U19D and becomes the X2CLK output. A second division by 2 is performed by U9B and the basic DS-1 frequency of 1.544 MHz is obtained. The $\overline{Q}$ output of U9B is inverted and buffered by U19C to form the X1CLK output. Reclocking of the U9B Q output with the Q output of U17A results in U17B outputs that are the same frequency as the U9B output but are displaced by one half a time slot. These outputs of U17B are designated Ø and $\overline{Ø}$. The $\overline{Ø}$ output is inverted and buffered by U11B and becomes the basic clock singal for use by the output modules.

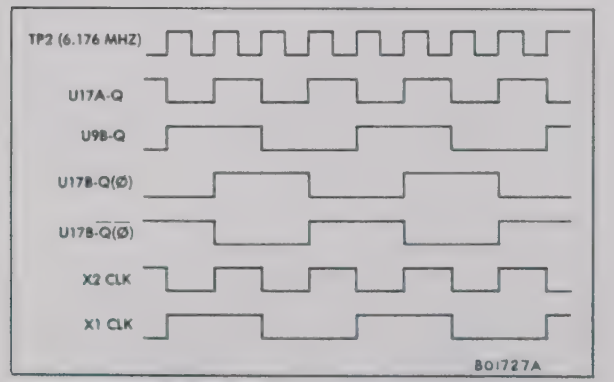


Figure 5—2. Oscillator And Clock Generator Timing Diagram

5.21 QRW GENERATOR.

5.22 The QRW (Quasi Random Word) generator produces a bit stream of logical ones and zeros that occur in a pattern long enough to appear to be quasi random in nature. Use of a 20-bit shift register and feedback decoding of bits b_{17} and b_{20} results in a pattern that repeats in frames of 1,048,575 bits at a basic rate of 1.544 megabits per second. The Ø clock, buffered by exclusive OR gate U4D (which also provides an inversion), is the clock input to shift registers U1, U2, and U3.

5.23 Bits b_{17} and b_{20} are exclusive ORed by U4A to provide the serial input for the first shift register. During normal operation, the output of U8B is low and the output of U4A is passed by U4B with no inversion to the serial input. Bit b_{20} has been selected to provide the output bit stream. During operation (other than the state where 15 or more zeros exist), the output of U8A is low and bit b_{20} is passed by exclusive OR U4C with no inversion. This is the QRW bit stream.

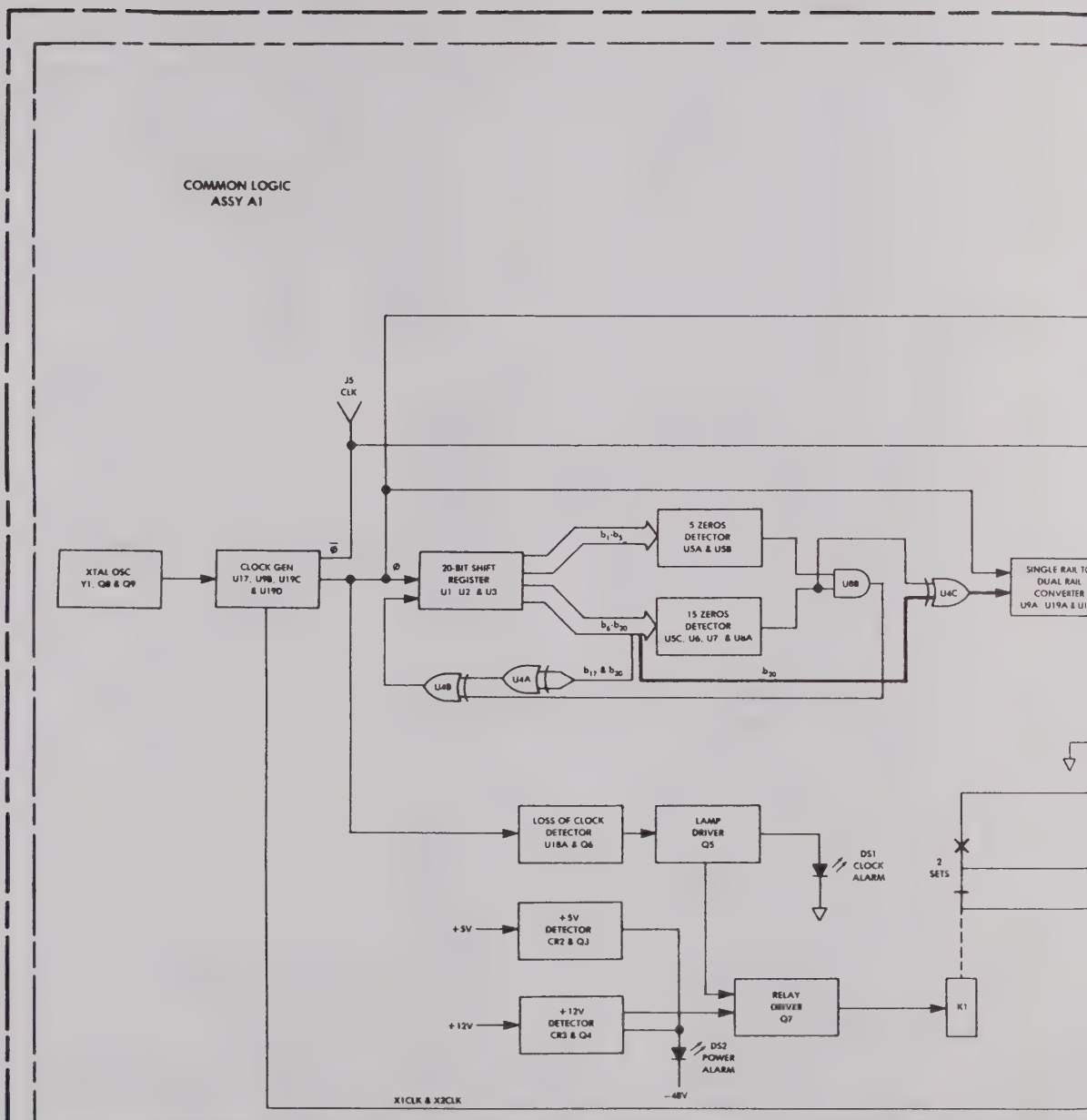
5.24 15 AND 20 ZERO DETECTORS.

5.25 The 15 and 20 zero detectors limit the number of successive zeros in the output bit stream to 14 and prevent the QRW generator from getting locked up in a non-operating mode at power on.

5.26 See Figure 5—3 for the timing diagram. Most of the time during normal operation at least one of the bits b_6 through b_{20} is high at any given time. Thus, at least one input to U8A is high, forcing the U8A output low. This allows bit b_{20} to pass through U4C and become the QRW bit stream. At other times, however, bits b_6 through b_{20} (or even bits b_2 through b_{20}) can all be low at the same time. Assuming the worst case where bits b_2 through b_{20} are low and bit b_1 is high, it would normally take 19 clock pulses to shift the high b_1 output to b_{20} so that a logical one is generated in the QRW bit stream. All of the intervening 19 time slots would result in zeros in the bit stream . . . clearly a violation of the 14 zero specification.

5.27 Assume bits b_6 through b_{20} are all low, and the four inputs of U8A are high, forcing U8A output high. It takes five time slots for the high b_1 to be shifted and appear as a high level at b_6. Thus the output of U8A will remain high for five time slots. During this time, b_{20} is low and the QRW output of U4C is forced high and represents five stuffed ones in the QRW bit stream. This will be followed by 14 successive zeros before the high b_6 is shifted to b_{20}, at which time another logical one will appear in the bit stream.

5.28 At the time power is first applied to the unit, it is possible for b_1 through b_{20} to all come up zeros. With no logical one appearing, it would never be possible for a logical one to be shifted into the shift register and operation would never start. To prevent this, a 20 zero detector is used.



COMMON EQUIPMENT MODULE

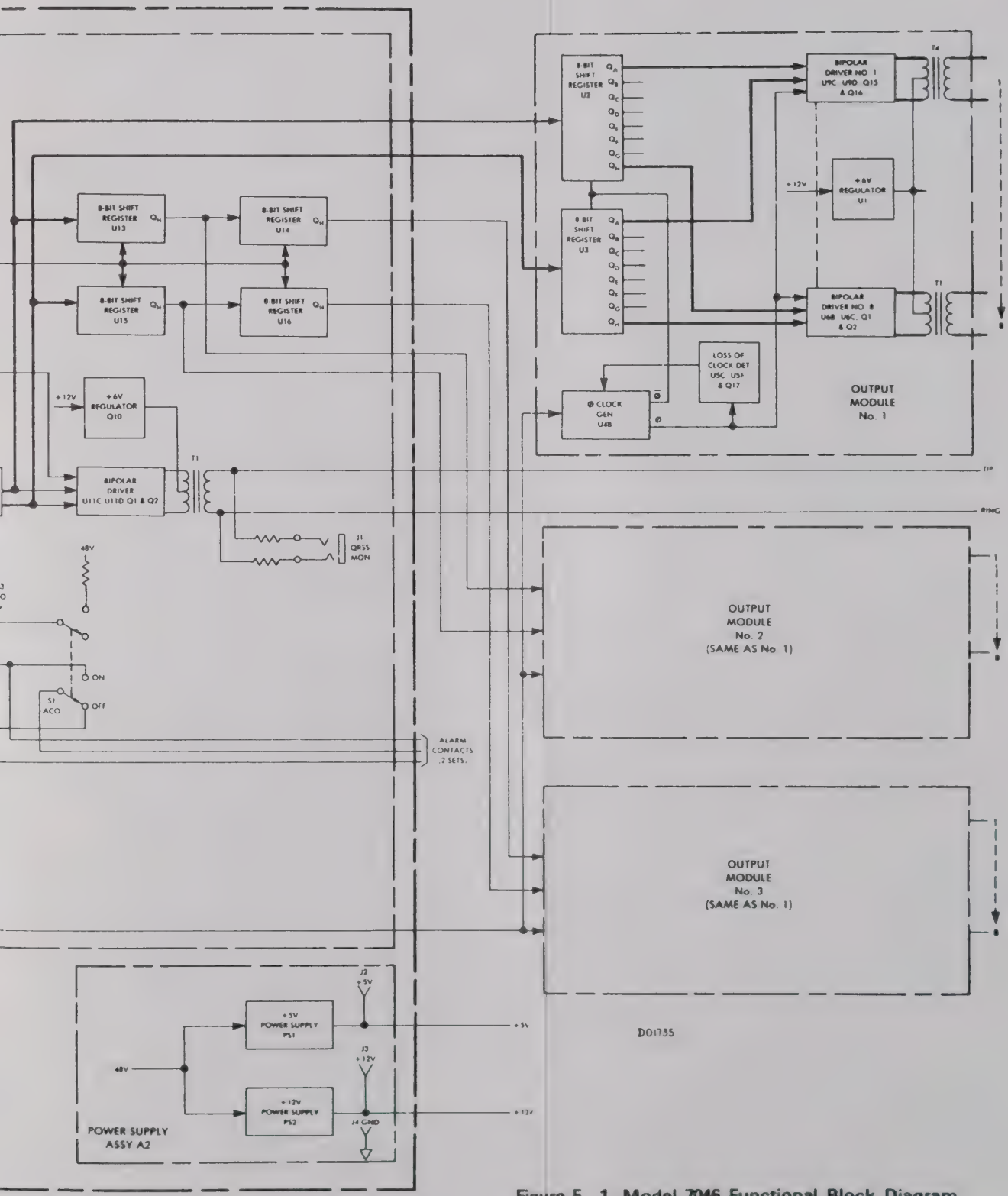


Figure 5—1. Model 7046 Functional Block Diagram

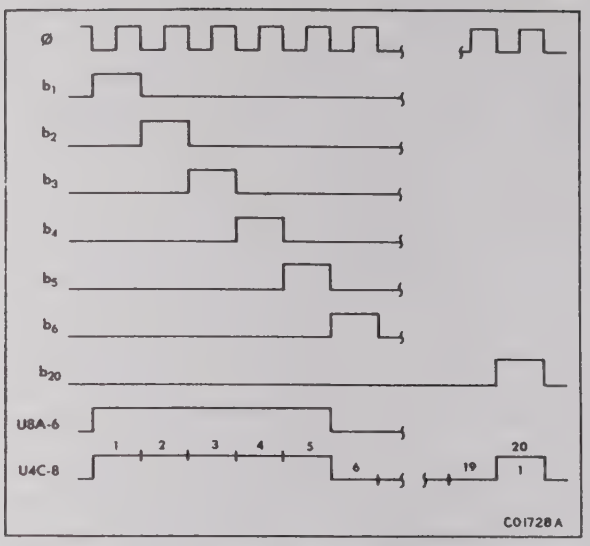


Figure 5—3. 15 Zero Detector Timing Diagram

5.29 Assuming that b_1 through b_{20} are all low, the outputs of U5A through U5C and U6A through U6C are high and the outputs of U7A through U7C are low. With the inversion provided by U6C, all inputs of U8A are high and the U8A output goes high. This insures that all inputs of U8B are also high. At this time, the output of U8B goes high and is applied to the serial input of U1 through U4B. The other input of U4B is low since b_{17} and b_{20} are both low at this time. The logical one shifted into the register ensures that the QRW generator will start and run properly.

5.30 SINGLE RAIL-TO-DOUBLE RAIL CONVERTER.

5.31 The QRW present at the output of U4C is referred to as a single rail signal, i.e., a single bit stream with all logical ones of the same positive polarity. In the final bipolar output bit stream of the unit, however, alternate ones must be of opposite polarity. The first step toward this end is to generate two bit streams, or a double rail signal, that has alternate ones appearing in two bit streams.

5.32 See Figure 5—4 for a timing diagram of the single rail-to-double rail converter. The QRW signal is applied to J-K flip flop U9A that toggles with the clock pulse when the QRW input is high and does not change when the QRW input is low. When the complementary outputs of U9A and the QRW signal are applied to U19A and U19B, the logical ones appear at a low level. U19A registers every other logical one and U19B the remainder. The signal is now in double rail format.

5.33 BIPOLAR OUTPUT NUMBER 1.

5.34 See Figure 5—5 for the timing diagram. The function of the bipolar output is to convert the double rail signal to a 6-volt peak-to-peak, bipolar output. The double rail signal is applied to U11C and U11D with the final clocking provided by $\overline{Ø}$. Logical ones in the double rail signal are low and occupy one complete time slot of 648 nanoseconds. When reclocked by $\overline{Ø}$, the logical ones are represented by a high level signal with a 50 percent duty cycle of 324 nanoseconds. Thus Q1 and Q2 are turned on by alternate logical ones and ground the respective ends of pulse transformer T1. With alternate ends of T1 being grounded, current flows through the primary first in one direction and then the other. This produces a bipolar output across the transformer secondary.

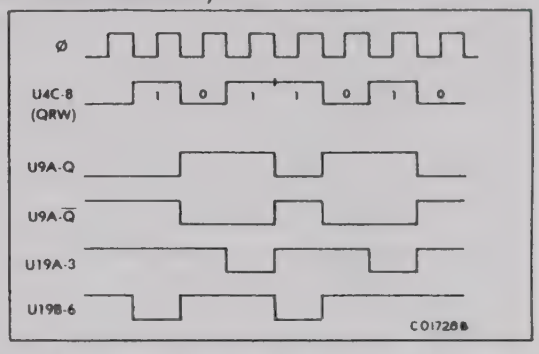


Figure 5—4. Single Rail-To-Double Rail Converter Timing Diagram

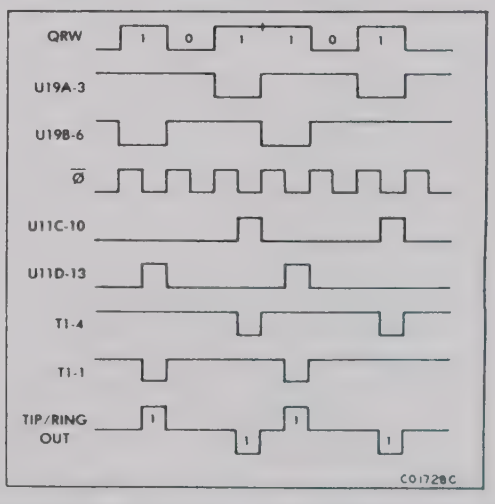


Figure 5—5 Bipolar Output No. 1 Timing Digaram

5.35 Emitter follower-type voltage regulator Q10 is adjusted to provide +6 Vdc at the center tap of T1. This sets the peak-to-peak output voltage to the desired level.

5.36 GROUP SHIFT REGISTERS.

5.37 See Figure 5—6 for the timing diagram. The group shift registers provide three double rail signal groups, each delayed from the other by eight time slots. The double rail signal at the outputs of U19A and U19B is applied to U12A and U12B and is clocked by $Ø$, which is applied uninverted through U7D. This delays the double rail signal one time slot with respect

to bipolar output number one. Shift register U13 delays the positive half of the double rail signal by eight time slots. An additional delay of eight time slots is provided by U14. The negative half of the double rail signal is delayed by U15 and U16. Thus three double rail signals, separated from each other by eight time slots, are generated. Before being applied to the output modules, the signals are buffered and inverted by U10A through U10F.

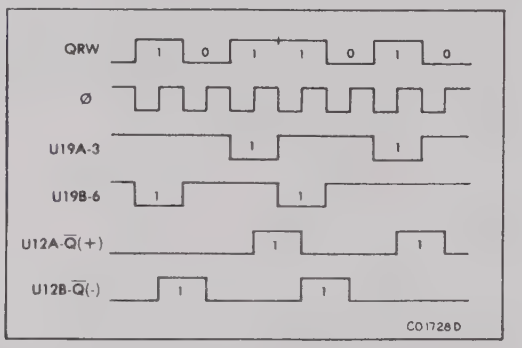


Figure 5—6. Group Shift Registers Timing Diagram

5.38 ALARM CIRCUITS.

5.39 Two alarm circuits are provided: (1) a loss-of-clock alarm, and (2) a loss-of-power alarm. Each circuit lights front panel indicators and provides two sets of relay contacts.

5.40 The loss-of-clock detector is U18A, a 30-microsecond, retriggerable one shot. Each negative transition of Ø retriggers the one shot and keeps the Q output continuously high. If the clock is lost for more than approximately 45 clock cycles, U18A times out; the U18A Q goes low and the $\overline{Q}$ goes high. Lamp driver Q5 turns on and CLOCK ALARM indicator DS1 is lighted. At the same time, the high $\overline{Q}$ output turns on Q6, which in turn, cuts off relay driver Q7. When alarm relay K1 is deenergized, the two sets of form C contacts alert the external alarm circuits.

5.41 The power alarm circuits will detect the loss (or lowering) of either the +5 Vdc or the +12 Vdc supplies, or when the 48 Vdc fuse blows. When the fuse blows the +5 Vdc that keeps K1 energized is lost, and the relay deenergizes, sounding the external alarm. At the same time, both Q3 and Q4 are turned on by the unfused −48 Vdc input and POWER ALARM indicator DS3 is lighted.

5.42 As long as the +5 Vdc and the +12 Vdc power supplies are functioning correctly, both Q3 and Q4 are cut off by small reverse biases developed across Zener diodes CR2 and CR3 respectively. When either the 5-volt supply drops below approximately +4 Vdc or the 12-volt supply below approximately +8.5 Vdc, Q3 or Q4 respectively is forward biased and turned on. This lights POWER ALARM DS2 and causes K1 to deenergize in one of two ways. If the +5 Vdc supply is faulty, K1 simply deenergizes and the alarm is sounded. If the +12 Vdc supply is faulty, the voltage at the junction of R9 and R15 drops below that required to keep Q7 turned on. This causes the alarm to be sounded.

5.43 To silence the external alarm during troubleshooting, ACO (Alarm CutOff) switch S1 is set to the ON position. This also lights ACO indicator DS3 as a reminder to maintenance personnel that the alarm system has been disabled.

5.44 POWER SUPPLIES.

5.45 Located on assembly A2 are the +5 Vdc and the +12 Vdc power supplies. These are non-repairable units. The −48 Vdc input furnished by the office is fused. Jacks J2 and J3 provide front panel points to monitor the supply voltages. Jack J2 is the ground reference.

5.46 **OUTPUT MODULE DETAILED CIRCUT DESCRIPTION.**

5.47 See Figure 7—6 for the schematic diagram of the 7046-40 output module. As shown on this illustration, an output module is comprised of a +6 Vdc power supply, a Ø clock generator, two shift registers, and eight identical bipolar output circuits.

5.48 +6 VDC POWER SUPPLY.

5.49 Voltage regulator U1 is a non-repairable unit that furnishes a +6 Vdc output. This determines the peak-to-peak output level of all bipolar signals. The regulated output is adjusted by R2.

5.50 Ø CLOCK GENERATOR.

5.51 The Ø clock generator produces a clock signal (designated Ø) that is the replica of X1CLK but delayed one quarter time slot. See Figure 5—7 for a timing diagram of this function. The X1CLK signal is applied to the D input of U4B, which is clocked by the X2CLK signal. the Ø and $\overline{Ø}$ outputs are then the desired new clock pulses.

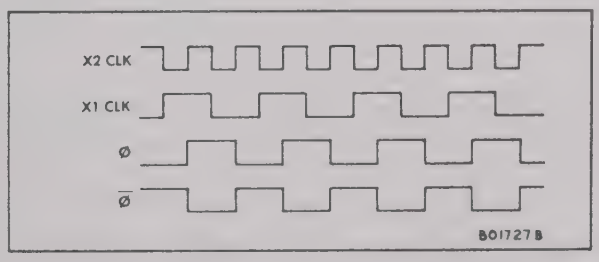


Figure 5—7. Ø Clock Generator Timing Diagram

5.52 An additional function of the Ø clock generator is to detect the loss of Ø clock. After an inversion by U5C, Ø is used to alternately turn Q17 on and off. When Q17 is cut off, C14 starts to charge toward +5 Vdc through R61. When Q17 is turned on, C14 is rapidly discharged through the transistor. As long as the clock is present, C14 never attains a charge large enough to cause the output of inverter U5F to go low. When the clock is lost, the final state of the Q output can be either high or low. If it is low, no further action is required. On the other hand if it is high, it must be set low so that all of the 16 transformer drivers are turned off for the protection of these devices. The high Q output is inverted by U5C and Q17 is cut off. Capacitor C14 rapidly charges to the supply voltage and the output of U5F goes low. This clears U4B and sets the U4B Q output low, which is the desired level.

5.53 SHIFT REGISTERS.

5.54 The shift registers provide eight sets of double rail signals such that each set is offset from its adjacent one by one time slot. The input to U3 is the + data and the input to U2 is the – data. Both of these, taken together, form the double rail signal. The + data input to U3 is shifted in by the positive transition of the $\bar{Ø}$ clock. Successive shifts produce levels at the Q_A through Q_H outputs that are the same as the input but delayed successively by one time slot each. See Figure 5–8 for a timing diagram. The – data is shifted in an identical manner by U2.

5.55 BIPOLAR OUTPUTS.

5.56 The eight identical bipolar output circuits are exactly the same as the number 1 bipolar ouptut described in paragraph 5.33. Although in this case the Ø clock is used to provide the final clocking, it is inverted by U5A-B and U5D-E and is equivalent to $\bar{Ø}$, the clock used for the number 1 bipolar output.

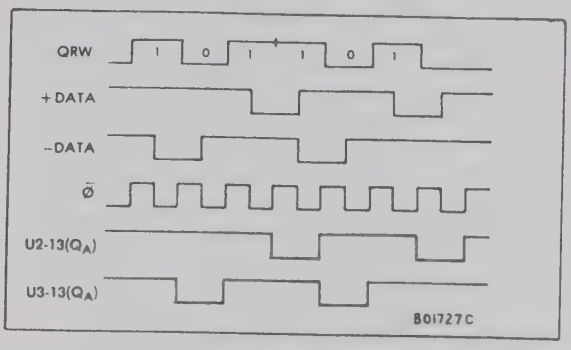


Figure 5–8. Shift Register Timing Diagram

SECTION 6

CALIBRATION

6.1 This section contains the instructions required to calibrate the basic clock frequency of 1.544 MHz and to set all outputs to 3.0±0.3 volts peak.

6.2 CLOCK FREQUENCY CALIBRATION.

6.3 To calibrate the 1.544 MHz clock output, perform the following steps.

1. Remove the 15 screws that secure the top cover and remove the cover.

2. Connect a frequency counter to CLK jack J5 and GND jack J4. See Figure 6–1.

3. On the common equipment module, adjust C1 to obtain a frequency counter indication of 1.544 MHz ±0.005%. See Figure 6–3.

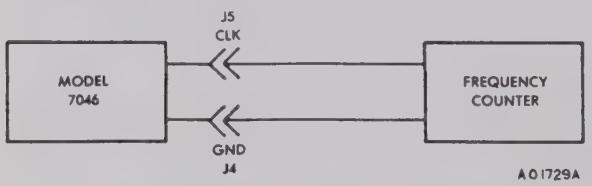


Figure 6–1. Model 7046 Clock Frequency Calibration Typical Test Setup.

6.4 OUTPUT NUMBER 1 LEVEL CALIBRATION.

6.5 To calibrate the number 1 output level of the common equipment module, perform the following steps.

1. Remove the 15 screws that secure the top cover and remove the cover.

2. At the rear panel of the common equipment module, terminate the tip/ring terminals with 100 ohms (if not already terminated).

3. Connect an oscilloscope across the 100/ohm resistor. See Figure 6–2.

4. Set the oscilloscope to the differential measurement mode.

5. On the common equipment module, adjust R10 to obtain a signal on the oscilloscope that is 3.0±0.3 volts peak when measured at the center of a pulse. See Figure 6–3.

6. Place a drop of glyptol on the potentiometer to secure the adjustment.

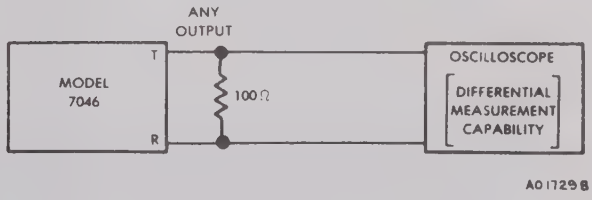


Figure 6–2. Model 7046 Output Level Calibration, Typical Test Setup.

6.6 OUTPUT MODULE LEVEL CALIBRATION.

6.7 To adjust the output level of any of the three output modules, perform the following steps.

1. Remove the 15 screws that secure the top cover and remove the cover.

2. At the rear of the output module to be calibrated, select any of the eight outputs and terminate it with 100 ohms (if not already terminated).

3. Connect an oscilloscope across the 100 ohm resistor. See Figure 6–2.

4. Set the oscilloscope to the differential measurement mode.

5. On the appropriate output module, adjust R2 to obtain a signal on the oscilloscope that is 3.0±0.3 volts peak when measured at the center of a pulse. See Figure 6–3.

6. Place a drop of glyptol on the potentiometer to secure the adjustment.

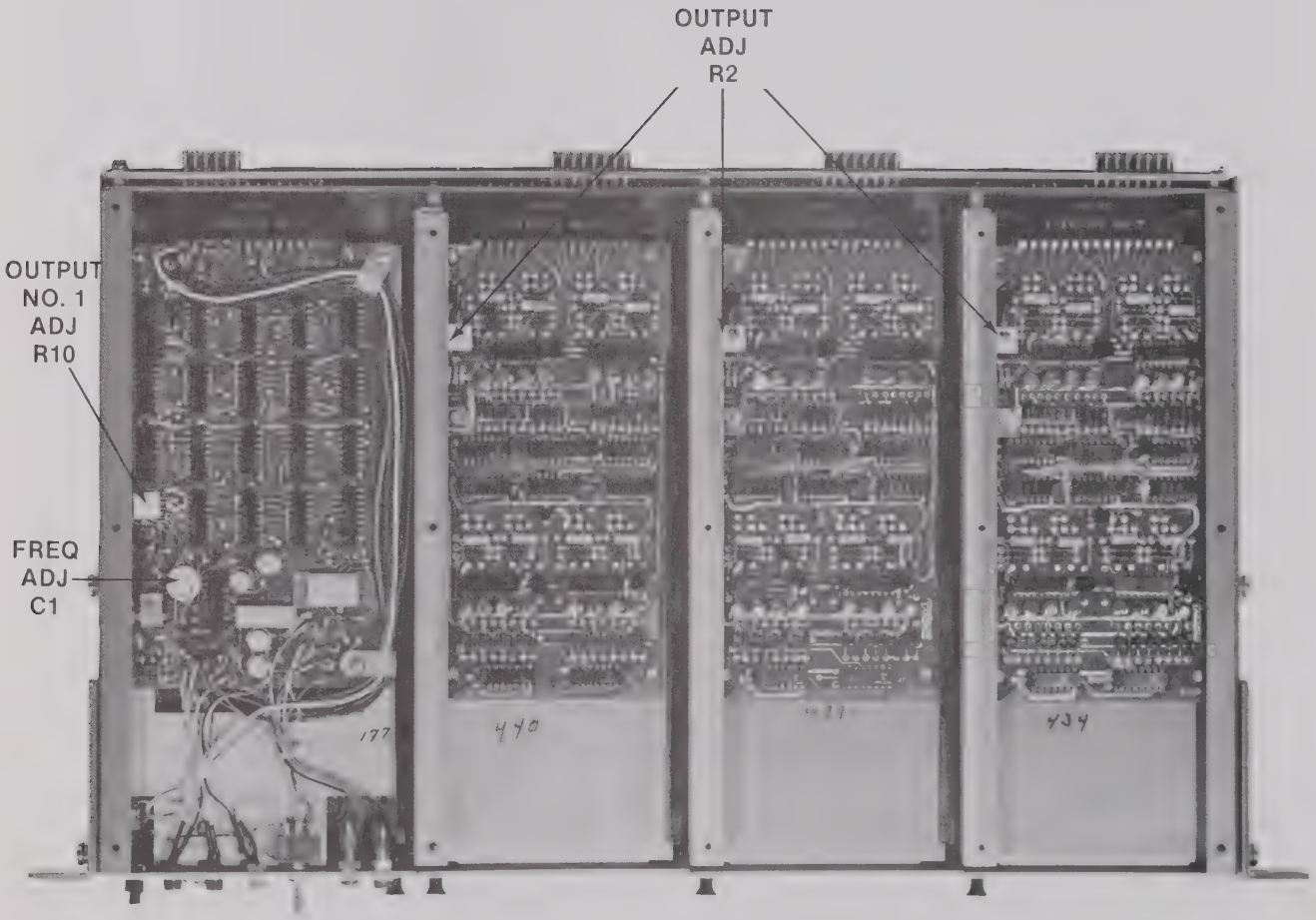


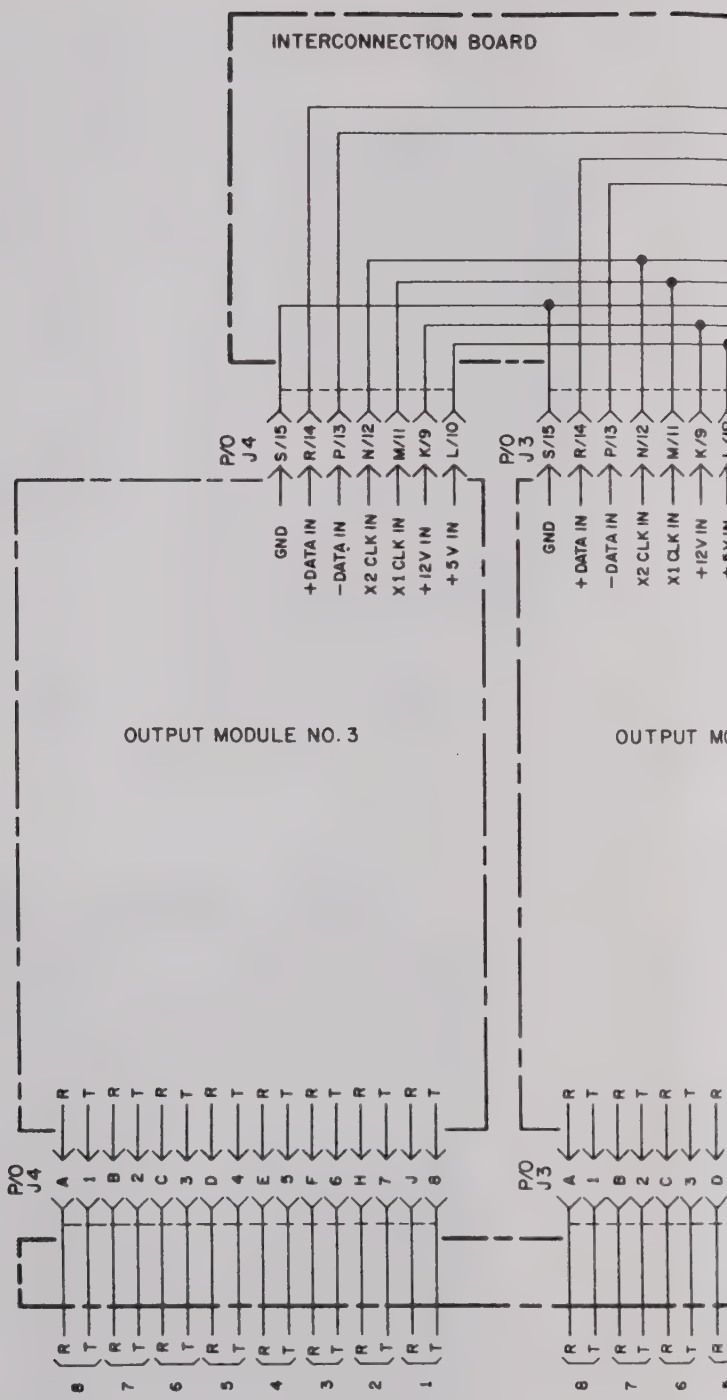
Figure 6—3. Model 7046 Calibration Adjustment Locations.

SECTION 7

DIAGRAMS

7.1 This section contains the schematic diagrams and the parts location diagrams for the 7046 series of equipment.

THIS PAGE LEFT INTENTIONALLY BLANK


INTERCONNECTION BOARD
P/O J4
S/15
R/14
P/13
N/12
M/11
K/9
L/10
GND
+DATA IN
−DATA IN
X2 CLK IN
X1 CLK IN
+12V IN
+5V IN
P/O J3
OUTPUT MODULE NO. 3
OUTPUT M
A
1
B
2
C
3
D
4
E
5
F
6
H
7
J
8
R
T

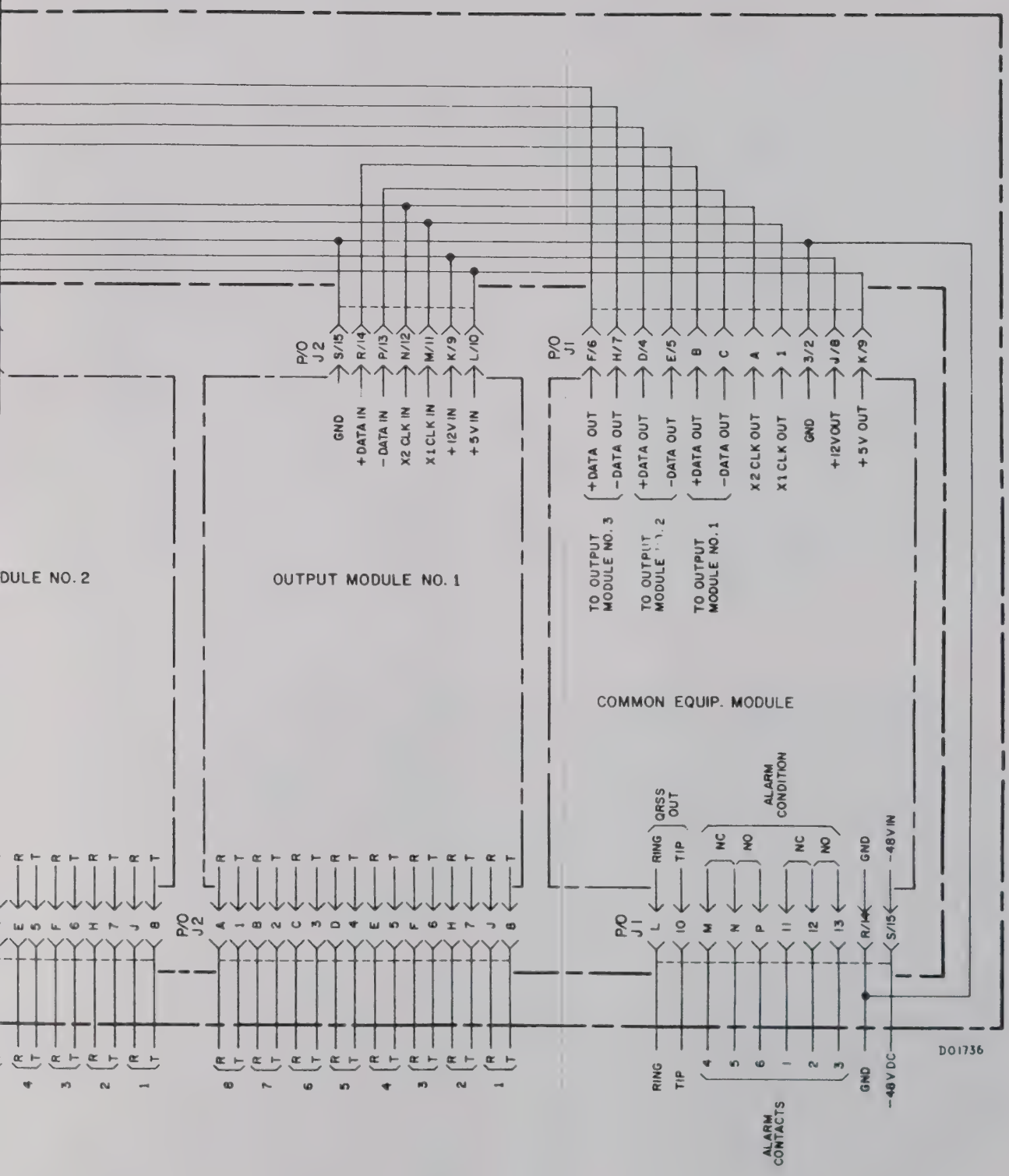


Figure 7—1. 7046 QRSS Generator Series Interconnection Diagram

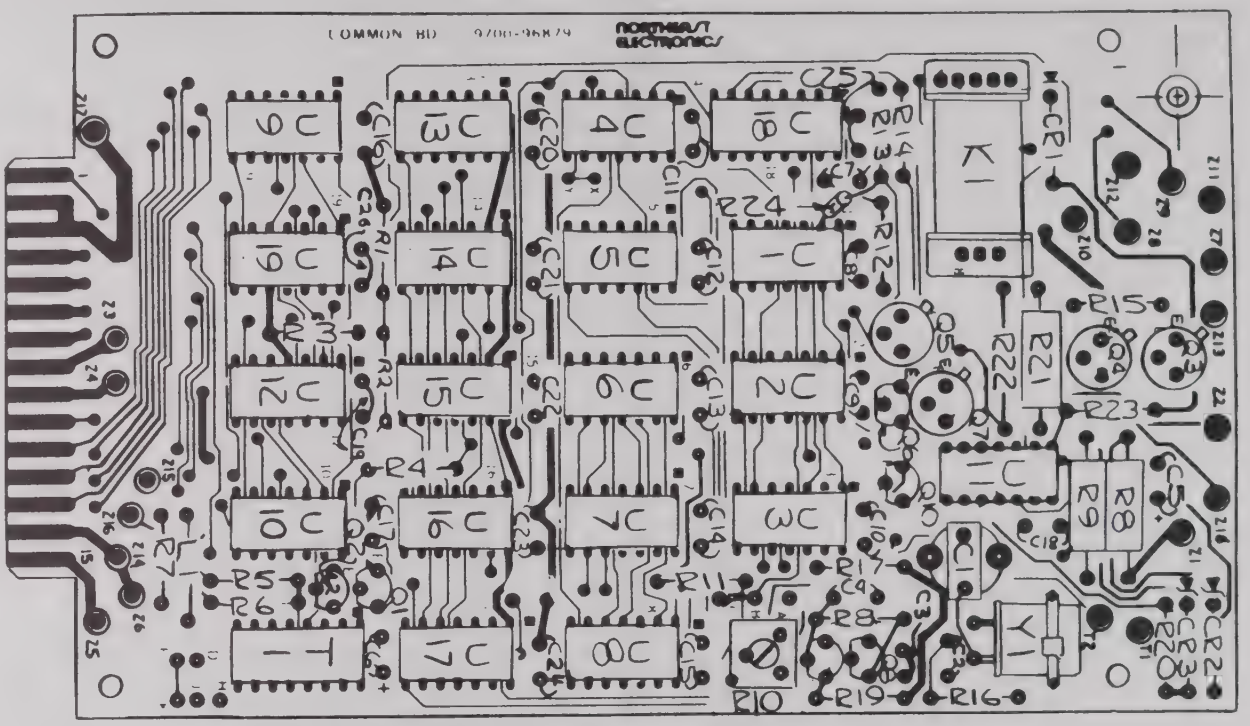


Figure 7—2. Common Logic Board A1, Component Location

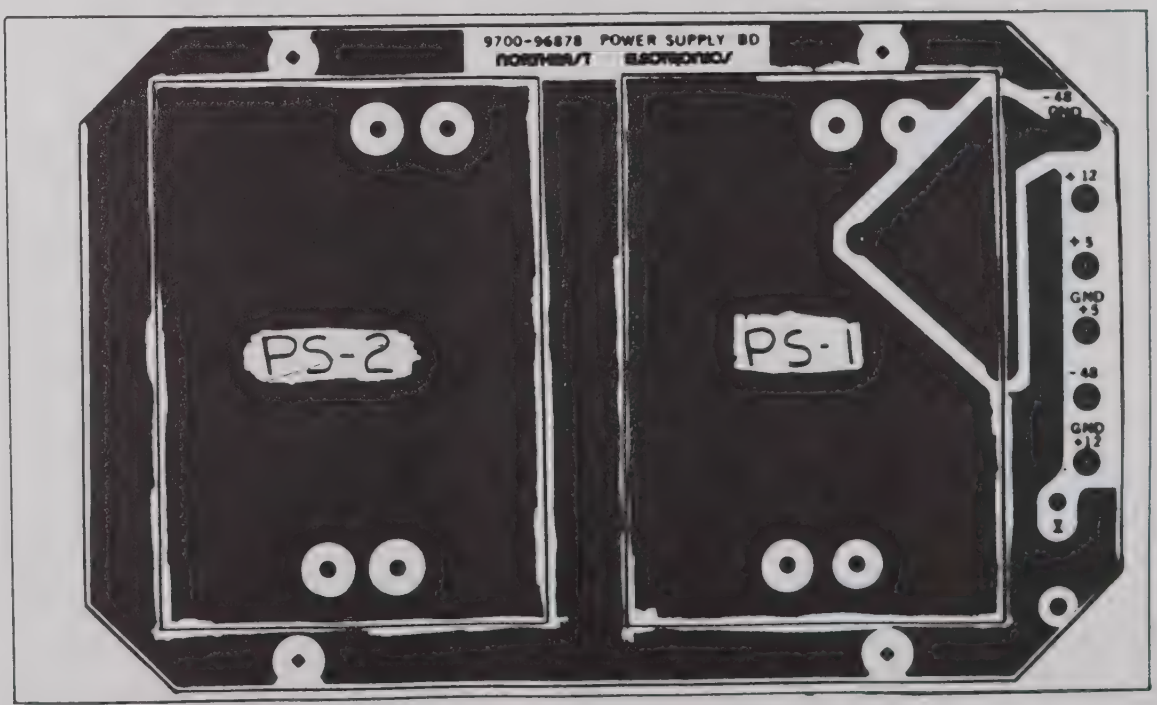
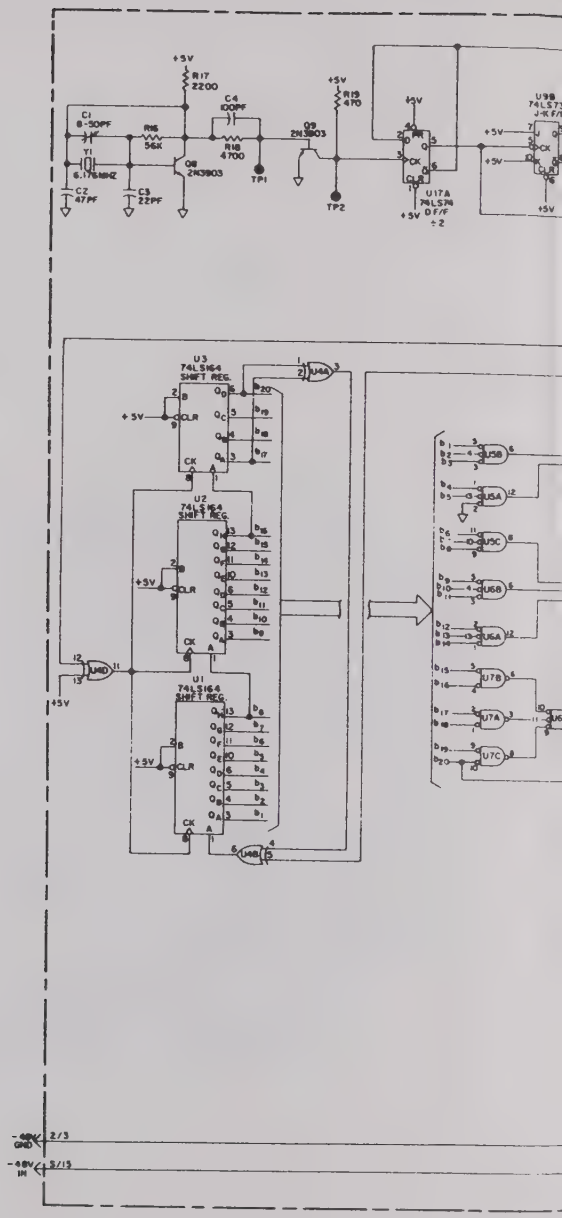


Figure 7—3. Power Supply Board A2, Component Location.

Figures 7—2/7—3



I C.	TYPE	PIN +5V	PIN GND	C
U1, U2, U3, U13, U14 U15, U16	74LS164	14	7	C8, C9 C10 C20
U4	74LS86	14	7	C
U5, U6	74LS27	14	7	C12
U7	74LS32	14	7	C
U8	74LS21	14	7	C
U9	74LS73	4	11	C
U10	74LS04	14	7	C
U11	74LS33	14	7	C
U12, U17	74LS74	14	7	C11
U18	9602	16	8	C
U19	74LS00	14	7	C

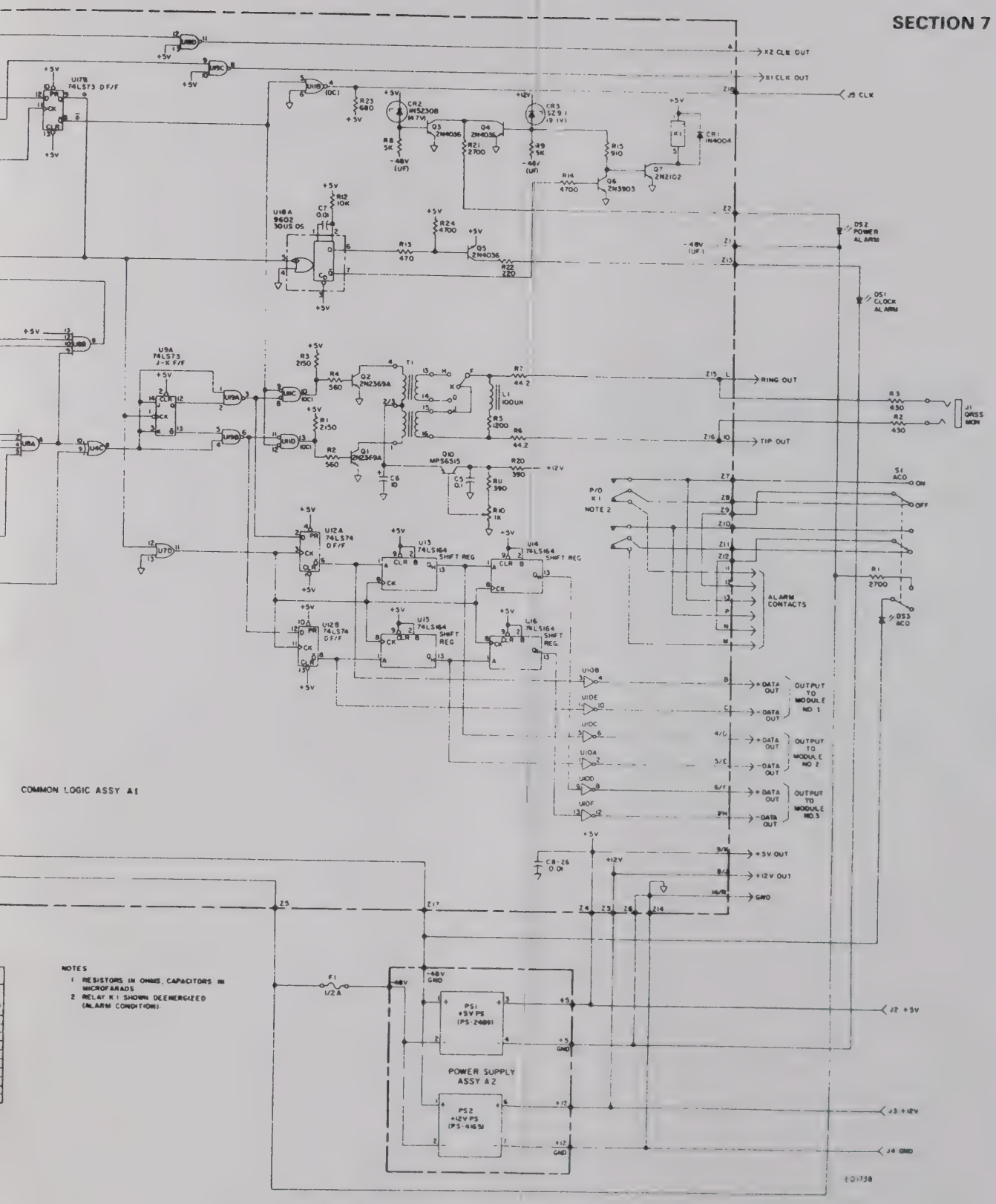
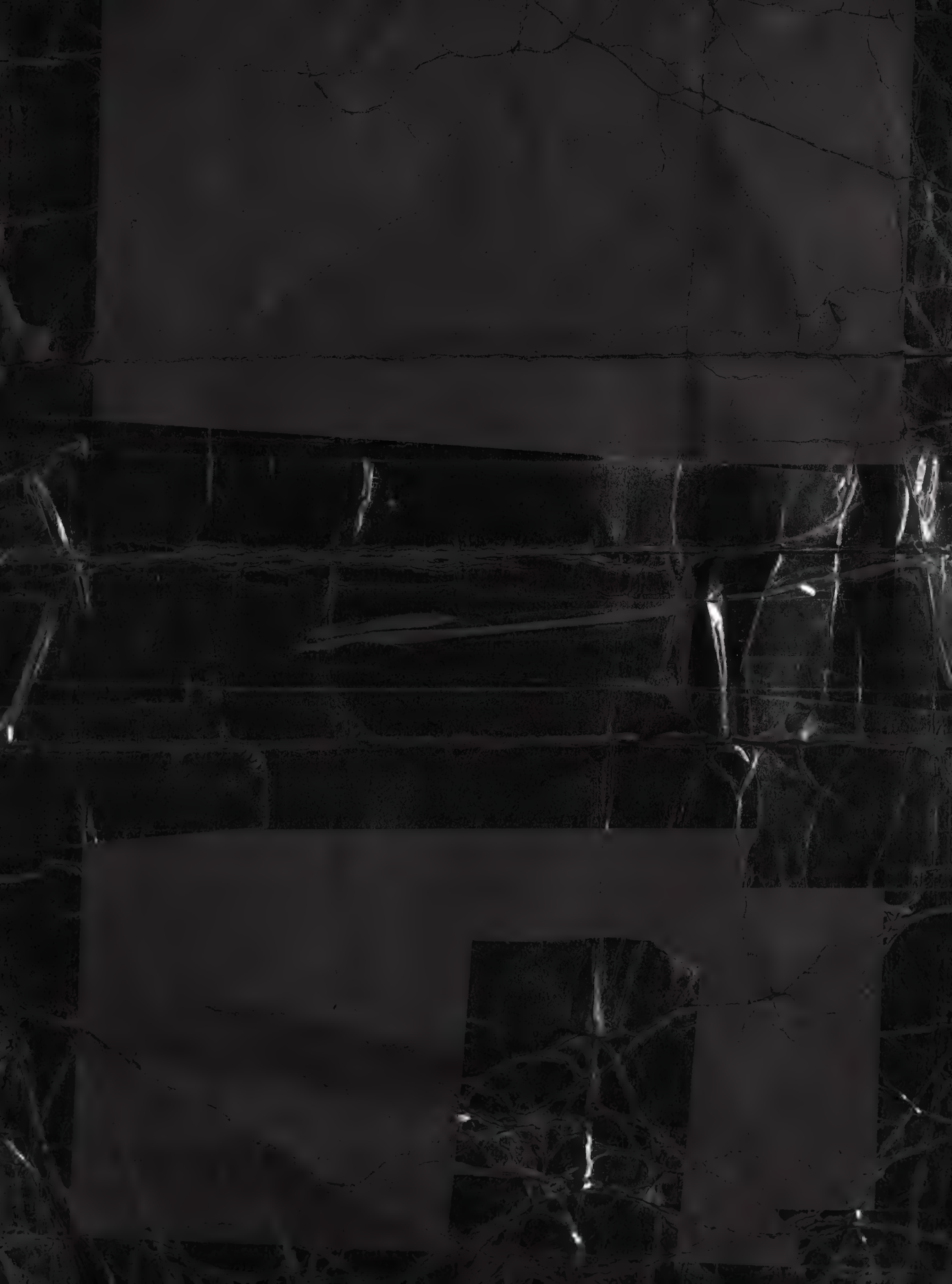

COMMON LOGIC ASSY A1
POWER SUPPLY ASSY A2
ALARM CONTACTS
OUTPUT TO MODULE NO 1
OUTPUT TO MODULE NO 2
OUTPUT TO MODULE NO 3
NOTES
1 RESISTORS IN OHMS, CAPACITORS IN MICROFARADS
2 RELAY K1 SHOWN DEENERGIZED (ALARM CONDITION).

Figure 7—4. 7046 Common Equipment Module, Schematic Diagram



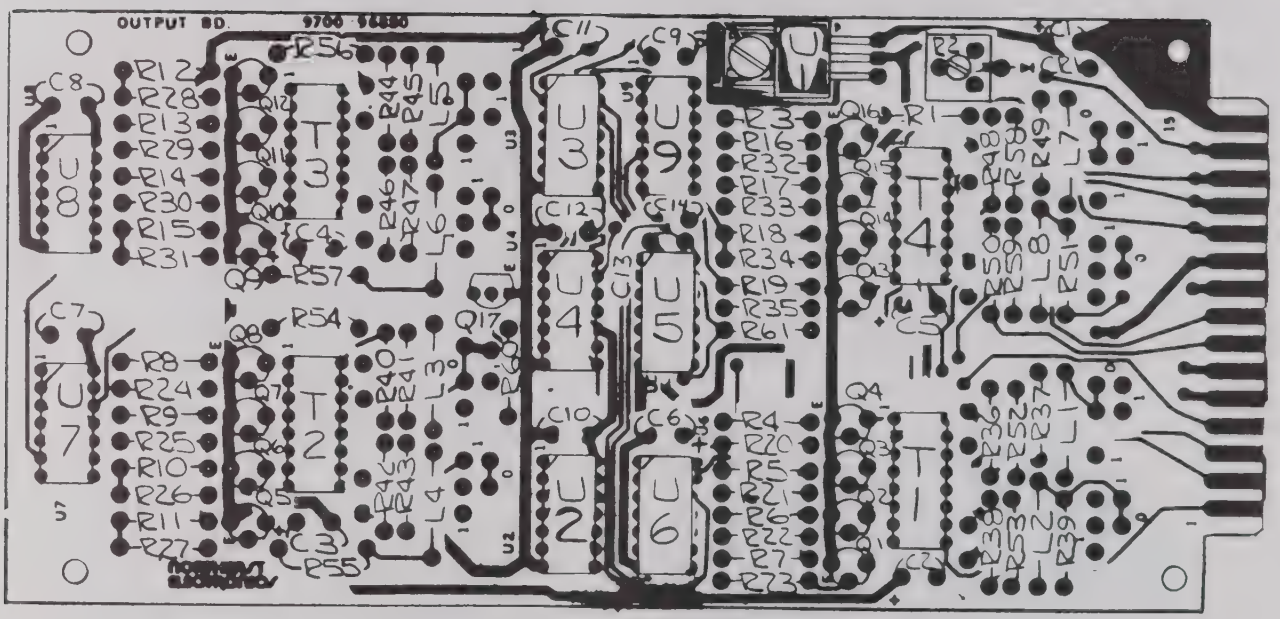
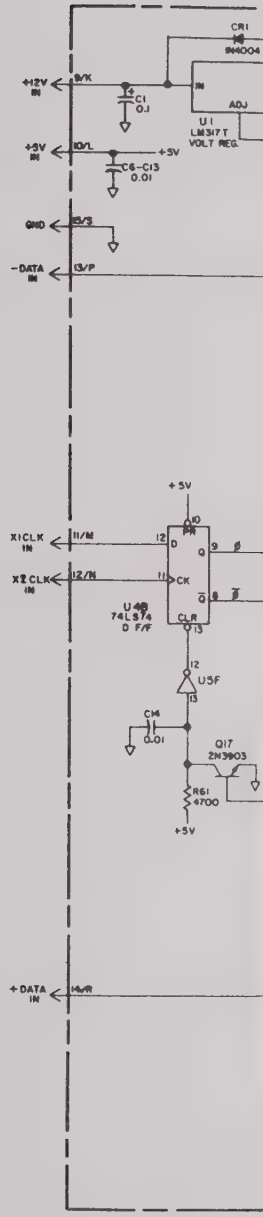
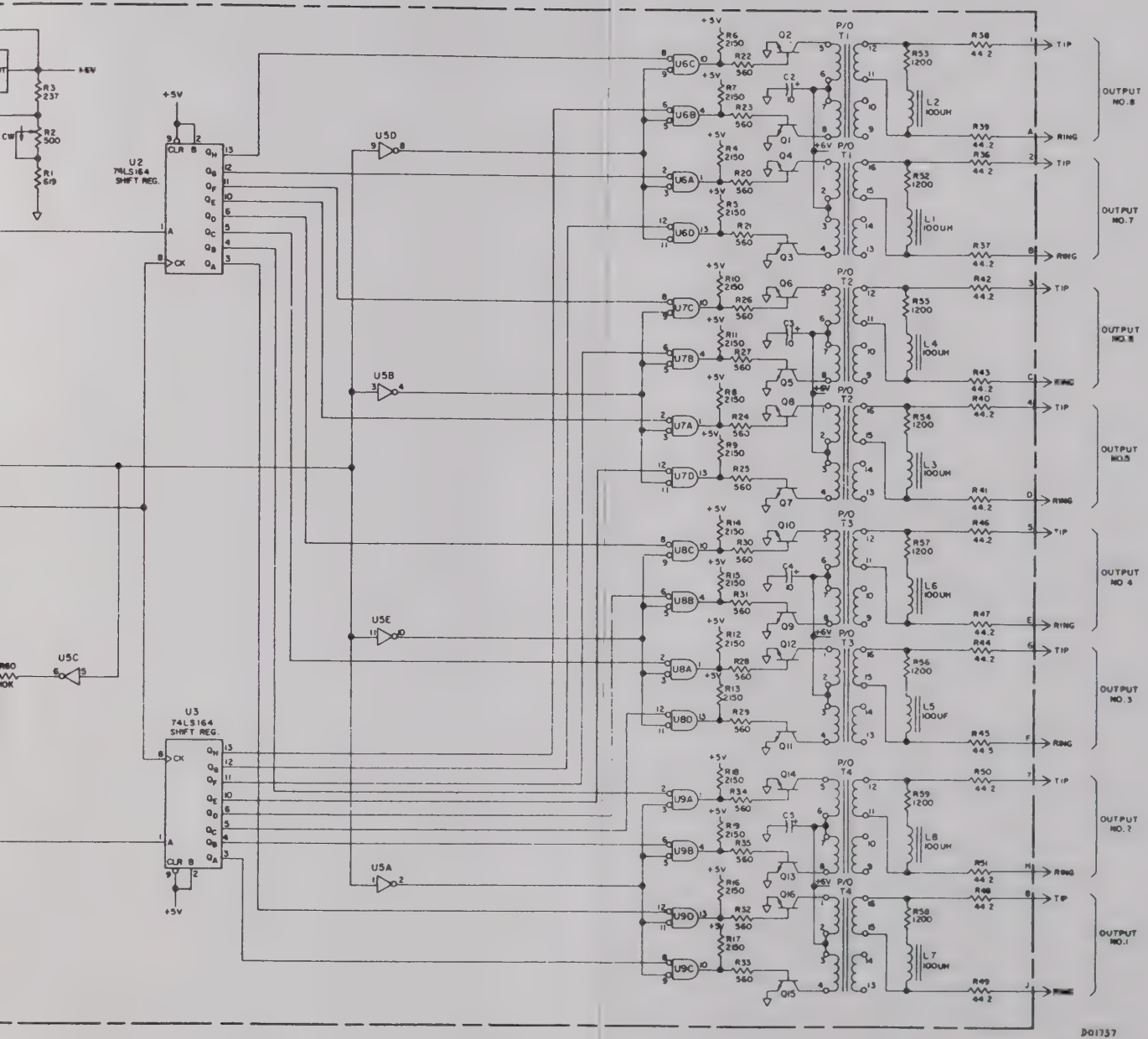


Figure 7—5. 7046-40 Output Module, Component Location

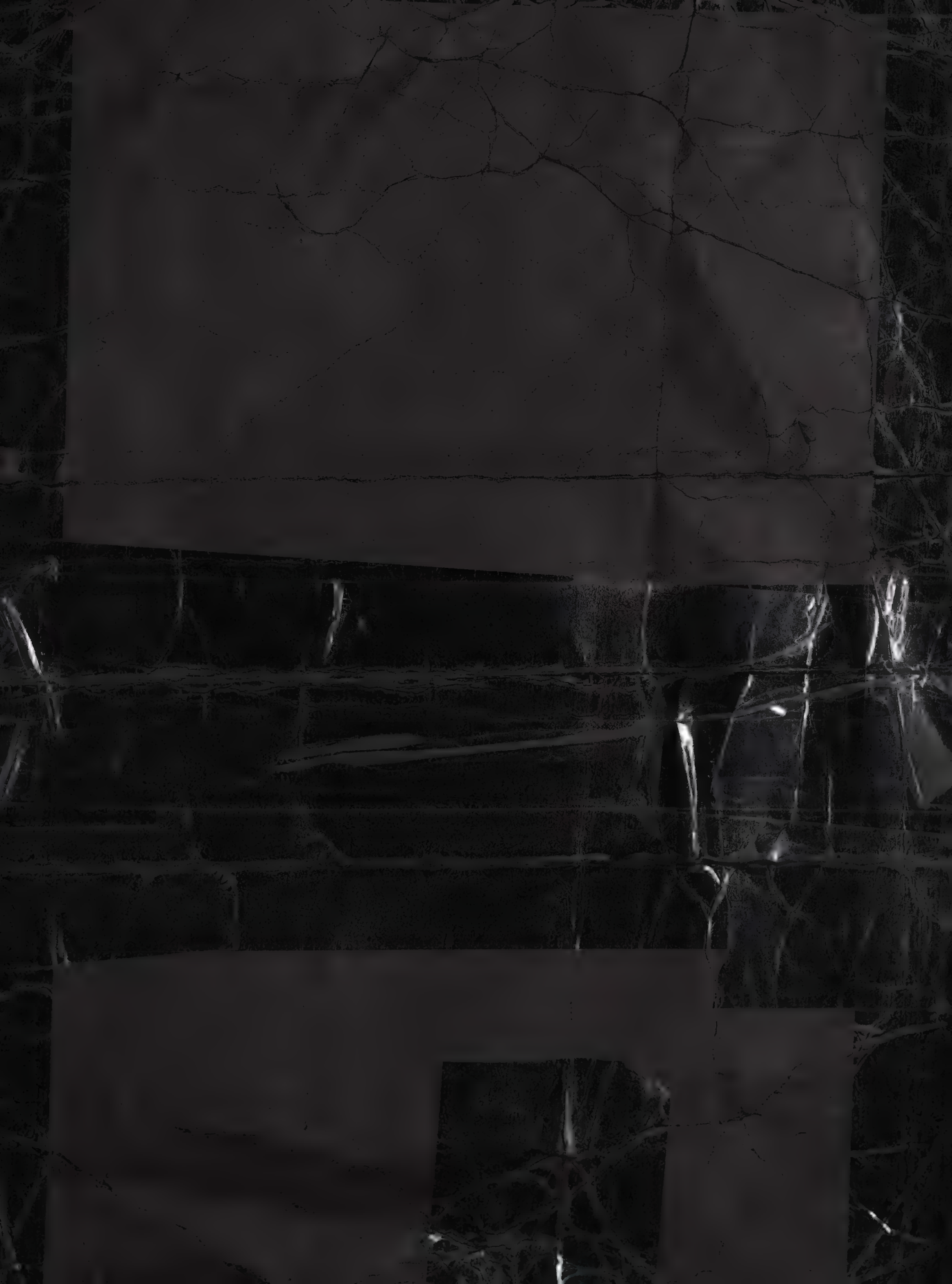

CR1
IN4004
+12V IN
9/K
C1 0.1
IN
ADJ
U1 LM317T VOLT REG.
+5V IN
10/L
+5V
C6-C13 0.01
GND
15/3
-DATA IN
13/P
+5V
X1CLK IN
11/M
12
D
Q
9
X2CLK IN
12/N
11
CK
U4B 74LS74 D F/F
CLR
13
12
U5F
13
C14 0.01
Q17 2N3903
R61 4700
+5V
+DATA IN
14/R



I.C	TYPE	PIN		CAP
		+5V	GND	
U2, U3	74LS164	14	7	C10, C11
U4	74LS74	14	7	C12
U5	74LS04	14	7	C13
U6 - U9	74LS33	14	7	C6 - C9

NOTES:
1. RESISTORS IN OHMS, CAPACITORS IN MICROFARADS.
2. UNLESS OTHERWISE INDICATED, TRANSISTORS ARE 2N2369A

Figure 7—6. 7046-40 Output Module Schematic Diagram



SECTION 8

ELECTRONIC PARTS LISTS

8.1 This section contains the electronic parts lists for the 7046 series of equipment.

Table 8—1. Common Equipment Module Overall Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
A1	PC ASSY 96878 PWR SUPPLY						A704600014
A2	PC ASSY 96879 COM LOGIC						A704600015
DS1-2		20 MA			H.PACKARD	5082-4655	564500802
DS3		20 MA			H.PACKARD	5082-4555	564500803
F1	1/2 A				NORTHERN	A0207849	862900001
J1				** NO FIXFLE **			620403100
J1	MT332B				SWCRFT	5J-1583	650403100
J2				** NO FIXFLE **			652800001
J2-3	TYPE 2	RED			EF JOHNSON	105-0202-200	652800003
J4	TEST JACK,BLK				RAYTHEON	TJ105BL	650600100
J5	TYPE 2	YELLOW			EF JOHNSON	105-0207-200	652800005
R1	2.7K	3W	10%		IRC	PW3	210302726
R2-3	430-	1/4W	5%		AB	TYPE CB	200104315
S1	3PDT	5A		28V	C+K COMP	7301P3H3ZB	620401200
XDS1-2	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-RTP	850501101
XDS3	LED MTG. CLIP FOR T1 3/4				VISUAL COM	CLF-280-YTP	850501103
XF1	FUSE BLOCK				NORTHERN	A0207307	863000401
XF1				** NO FIXFLE **			863400401

Table 8—2. Common Logic Board A1 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	8-50PF			350V	ERIE	557-091E-8-50	340005000
C2	47PF		5%	100V	ELMENCO	CM04-A470J0-	335404700
C3	20PF		5%	100V	ELMENCO	CM04EA200JO	335402000
C4	100PF	DB N3300	10%	1KV	CENTRALAB	DD-101	330001010
C5	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C6	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C7-26	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1	D041	1A	SI	400V	EDAL	IN4004	560040040
CR2	D07	500MW	5%	4.7V	MOTOROLA	1N5230B	562052300
CR3	A140	1W	1%	9.1V	SCHAUER	SZ9.1	562000910
K1	RELAY REED 2CPC				MIDTEX	172-100BA9	604105600
L1	100UH		5%		NYTRONICS	WEE-100	461000600
Q1-2	TO-18	360MW TA	NPN	15V	FAIRCHILD	2N2369A	550023691
Q3-5	TO5	7W TA	PNP	65V	RCA	2N4036	552040360
Q6	TO-92	350MW TA	NPN	40V	MOTOROLA	2N3903	550039030
Q7	TO-5	1W TA	NPN	65V	RCA	2N2102	550021020
Q8-9	TO-92	350MW TA	NPN	40V	MOTOROLA	2N3903	550039030
Q10	TO-92	350MW TA	NPN	25V	MOTOROLA	MPS6515	550065150
R1	2150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221511
R2	560-	1/4W	10%		AB	TYPE CB	200105616
R3	2150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221511
R4	560-	1/4W	10%		AB	TYPE CB	200105616
R5	1.2K	1/4W	10%		AB	TYPE CB	200101226
R6-7	44.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244291
R8-9	5K	3W	5%		W LEONARD	TYPE 3X	210305025
R10	1K	1/2W	10%	200V	HELIPOT	72PMR1K	232701022
R11	390-	1/4W	10%		AB	TYPE CB	200103916
R12	10K	1/4W	10%		AB	TYPE CB	200101036
R13	470-	1/4W	10%		AB	TYPE CB	200104716
R14	4.7K	1/4W	10%		AB	TYPE CB	200104726
R15	910-	1/4W	5%		A.B.	TYPE CB	200109115
R16	56K	1/4W	10%		AB	TYPE CB	200105636
R17	2.2K	1/4W	10%		AB	TYPE CB	200102226
R18	4.7K	1/4W	10%		AB	TYPE CB	200104726
R19	470-	1/4W	10%		AB	TYPE CB	200104716
R20	390-	1/2W	10%		AB	TYPE EB	200203916
R21	2.7K	3W	10%		IRC	PW3	210302726
R22	220-	1/4W	10%		AB	TYPE CB	200102216
R23	680-	1/4W	10%		AB	TYPE CB	200106816
R24	4.7K	1/4W	10%		AB	TYPE CB	200104726
T1	16DILP				ARTTED	AC8326	440200100
U1-3	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U4	14 DIP-P			LS	T.I.	SN74LS86N	510907486
U5-6	14 DIP-P			LS	T.I.	SN74LS27N	510907427
U7	14 DIP-P			LS	T.I.	SN74LS32N	510907432
U8	14 DIP-P			LS	T.I.	SN74LS21N	510907421
U9	14 DIP-P			LS	TI	SN74LS73N	510907473
U10	14 DIP-P				T.I.	SN74LS04N	510907404
U11	14 DIP-P			LS	T.I.	SN74LS33N	510907433
U12	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U13-16	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U17	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U18	16DIP-P			DM3	FAIRCHILD	9602PC	510096025
U19	14 DIP-P			LS	T.I.	SN74LS00N	510907400
Y1	CRYSTAL,6.176MHZ				VALPEY	6.176MHZ-VM6	919100005

Table 8—3. Power Supply Board A2 Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
PS1	Q 5V OUT	1 AMP			S.-ARNOLD	PS-2489	960100006
PS2	Q12V OUT	.400 AMP			S.-ARNOLD	PS-4165	960100005

Table 8—4. Mother Board Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
J1-4	15DILP				AMP	582783-3	651902100

Table 8—5. Output Module Parts List

REFERENCE DESIGNATOR	DESCRIPTION VALUE	POWER	TOL	VOLTS	MFGR.	MFGR. PART NO.	N.E. PART NO.
C1	.1UF		10%	35V	KEMET	T330A104K035AS	310001041
C2-6	10UF		10%	10V	KEMET	T330A106K010AS	310001060
C7-14	.01UF		20%	16V	CENTRALAB	UK16-103	330701031
CR1	D041	1A	SI	400V	EDAL	IN4004	560040040
L1-8	100UH		5%		NYTRONICS	WEE-100	461000600
Q1-16	TO-18	360MW TA	NPN	15V	FAIRCHILD	2N2369A	550023691
Q17	TO-92	350MW TA	NPN	40V	MOTOROLA	2N3903	550039030
R1	619-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220261901
R2	500-	1/2W	10%	200V	HELIPOT	72PMR500	232705010
R3	237-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220223701
R4-19	2150-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220221511
R20-35	560-	1/4W	10%		AB	TYPE CB	200105616
R36-51	44.2-	1/8W	1%		ELECTRA	RN55 SIZE 100 PPM	220244291
R52-59	1.2K	1/4W	10%		AB	TYPE CB	200101226
R60	10K	1/4W	10%		AB	TYPE CB	200101036
R61	4.7K	1/4W	10%		AB	TYPE CB	200104726
T1-4	16DILP				ARTTED	AC8326	440200100
U1	TO-220				NATIONAL	LM317 T	500000317
U2-3	14 DIP-P			LS	T.I.	SN74LS164N	510974164
U4	14 DIP-P			LS	T.I.	SN74LS74N	510907474
U5	14 DIP-P				T.I.	SN74LS04N	510907404
U6-9	14 DIP-P			LS	T.I.	SN74LS33N	510907433

FOR FUTURE UPDATES

If you want to receive updates or revised issues of this manual, please complete and mail the postage paid card below. *If you fail to do so, important updated information pertaining to this document will not be forwarded to you.*

If you would like a representative to call, require additional information on Tau-tron products, or would like to be placed on our mailing list, please complete and mail the *lower* postage paid card.

Instruction Manual Form Number [ ][ ][ ][ ][ ]–[ ][ ][ ][ ][ ]

☐ Yes, I would like to receive technical updates and revised issues of this document. I have filled in the manual form number above (Part No. is shown on title page).

to: Publications Manager
from:

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State & Zip _____ Phone _____

Comments _____

_____

Please —

☐ Have representative call.

☐ Add me to your mailing list.

Send additional information on:

☐ Bit Error Rate Testing
☐ TDM Voice/Data Multiplexers
☐ Digital Transmission Test Sets
☐ Data Loggers
☐ High Speed Components

My general application is _____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State & Zip _____ Phone _____

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY CARD
FIRST CLASS PERMIT NO. 19 WESTFORD, MA

ATTN: Publications Manager

Tau-tron Inc.

10 Lyberty Way
Westford, MA. 01886

NO POSTAGE
NECESSARY
IF MAILED

BUSINESS REPLY CARD

ATTN: Sales Department

Tau-tron Inc.

10 Lyberty Way
Westford, MA. 01886

Repair Returns

To return a unit for repair:

1. Call the Customer Service Dept. **(508) 692-5100** or **1-800-TAU-TRON (outside MA),** for a **Repair Authorization Number.** This will reduce administrative delays and ensure prompt return of your unit.
2. Complete and **attach one of the Repair Tags** below to your unit.
3. **Pack the unit** in the original shipping carton and packaging materials, if available. Otherwise use a double-walled carton (test strength of 350 lb) and shock absorbing material such as bubble wrap to prevent the unit from moving in the carton during transit. Seal with heavy paper tape.
4. **Send to:**

   Tau-tron
   10 Lyberty Way
   Westford, MA 01886
   attn: Customer Service

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

Form 0163-1181 A

Repair Tag

Repair Authorization Number _____

Model _____ **Serial Number** _____

☐ Warranty repair ☐ Dead on arrival ☐ Repair ☐ Modification ☐ Recalibration

Symptoms: _____

_____

Name _____ Title _____

Company _____ Dept./MS _____

Address _____ City _____

State&Zip _____ Phone _____

tau-tron

A UNIT OF

GENERAL SIGNAL

TAU-TRON INC.
10 LYBERTY WAY, WESTFORD, MA 01886
(508) 692-5100 1-800-TAU-TRON (Outside MA)
Telex 750245 FAX 508-692-1938